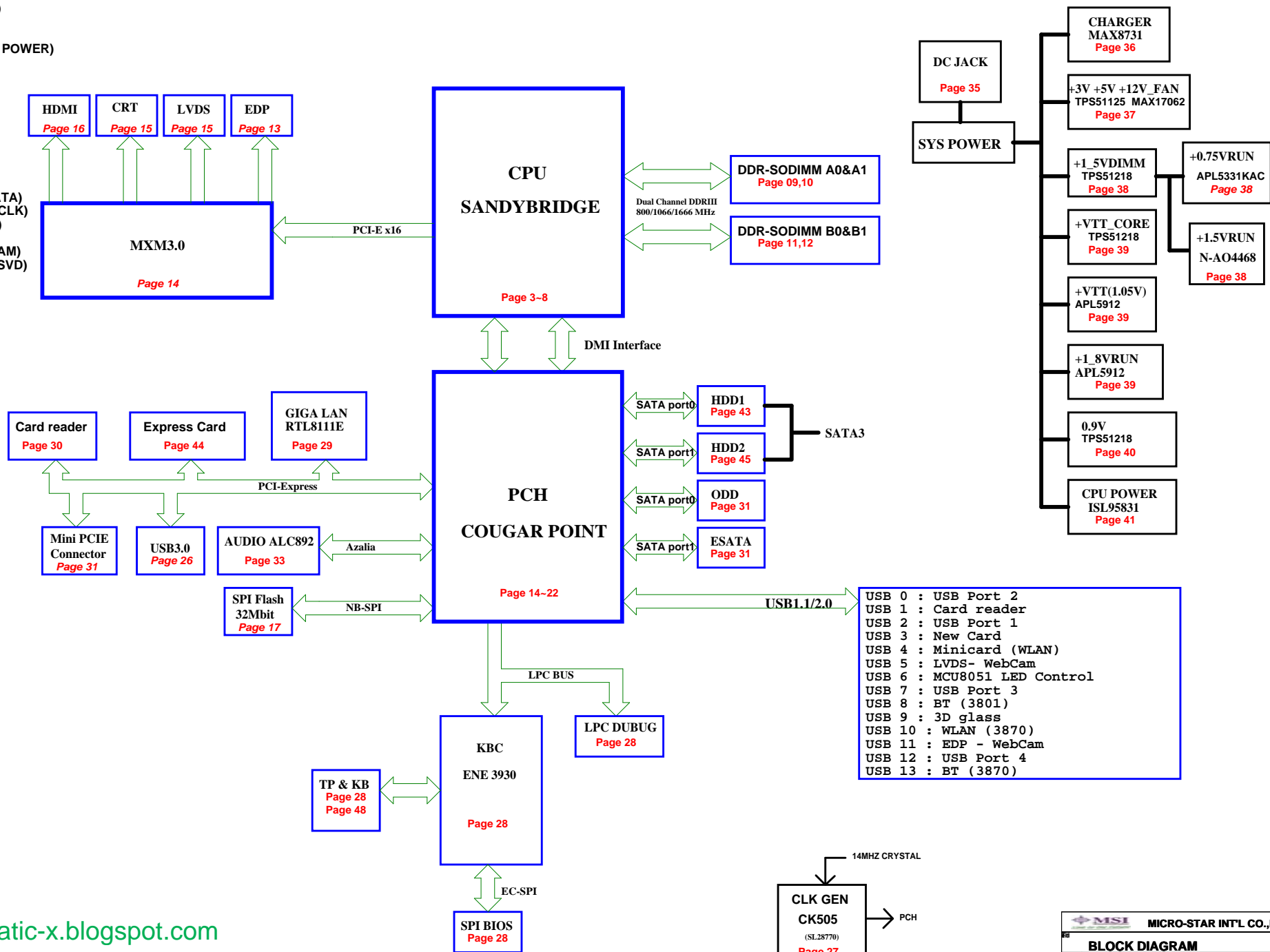


## Huron River Platform

- 01 : BLOCK DIAGRAM  
 02 : PLATFORM  
 03 : PROCESSOR-1 (HOST BUS)  
 04 : PROCESSOR-2 (DDR3)  
 05 : PROCESSOR-3 (POWER)  
 06 : PROCESSOR-4 (GRAPHICS POWER)  
 07 : PROCESSOR-5 (GND)  
 08 : PROCESSOR-6 (RESERVE)  
 09 : DDR3 SODIMM A0  
 10 : DDR3 SODIMM A1  
 11 : DDR3 SODIMM B0  
 12 : DDR3 SODIMM B1  
 13 : EDP  
 14 : MXM3.0 Slot  
 15 : CRT/LVDS/CCD  
 16 : HDMI  
 17 : CougarPoint (HDA/JTAG/SATA)  
 18 : CougarPoint (PCI-E/SMBUS/CLK)  
 19 : CougarPoint (DMI/FDI/GPIO)  
 20 : CougarPoint (LVDS/DDI)  
 21 : CougarPoint (PCI/USB/NVRAM)  
 22 : CougarPoint (GPIO/NCTF/RSVD)  
 23 : CougarPoint (POWER)  
 24 : CougarPoint (POWER)  
 25 : CougarPoint (GND)  
 26 : USB3.0(UPD720200)  
 27 : CLOCK GEN (SL28770)  
 28 : KBC/EC/uP (KB3930)  
 29 : GIGA LAN (RTL8111E)  
 30 : Card Reader (RTL5139)  
 31 : WLAN/TP/BTB/USB  
 32 : HDD2/ODD/ESATA /FAN/BT  
 33 : AUDIO(ALC892)  
 34 : LED\_EPF021J  
 35 : M\_Battery select  
 36 : M\_Battery Charger  
 37 : M\_System Power  
 38 : M\_DIMM\_1.5VRUN  
 39 : M\_VTT\_1.8VRUN  
 40 : 0.9V Power  
 41 : CPU Power  
 42 : EMI/Screw  
 43 : Test Pad  
 44 : 16F1A\_NewCard/HDD1  
 45 : 16F1B\_IO/Audio Board  
 46 : 16F1C\_HDD2  
 47 : 16F1D\_Cap Sensor Board  
 48 : 16F1E\_Touch Pad L/R Key  
 49 : 16F1F\_CDLED\_RF  
 50 : 16F1G\_ABLED Front  
 51 : 16F1H\_ABLED\_L  
 52 : 16F1I\_ABLED\_R  
 53 : 16F1J\_CDLED\_L  
 54 : 16F1K\_CDLED\_LF  
 55 : PowerDown Sequence  
 56 : PowerOn Sequence  
 57 : History



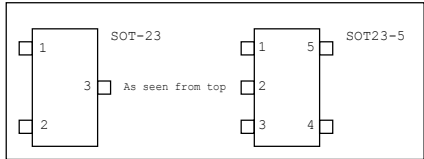
SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

Voltage Rails			
POWER PLANE	VOLTAGE	ACTIVE IN	DESCRIPTION
PWR_SRC	12V	S0, (S3-S5)	
+5VALW	5V	S0, (S3-S5)	
+5VRUN	5V	S0, S3	
+5VSUS	5V	S0	
+3VALW	3.3V	S0, (S3-S5)	
+3VRUN CK505	3.3V	S0	Clock, MCH
+3VSUS	3.3V	S0, S3	
+3VRUN	3.3V	S0	
+1_5VDIMM	1.5V	S0, (S3-S4)	DDR core
+1_5VSUS	1.5V	S0	
+1_5VRUN	1.5V	S0	
VTT	1.05V	S0	PCH
+0_75VRUN	0.75V	S0	DDR command & control pull up.
+VCC_CORE	1.05V-1.1V	S0	CPU core rail
+VCC_GFXCORE	1.1V	S0	GMCH Graphics core rail

Net Naming Conventions

Suffix
# = Active Low Signal
Prefix
H = Host
M = DDR Memory
TP = Test Point (does not connect anywhere else)

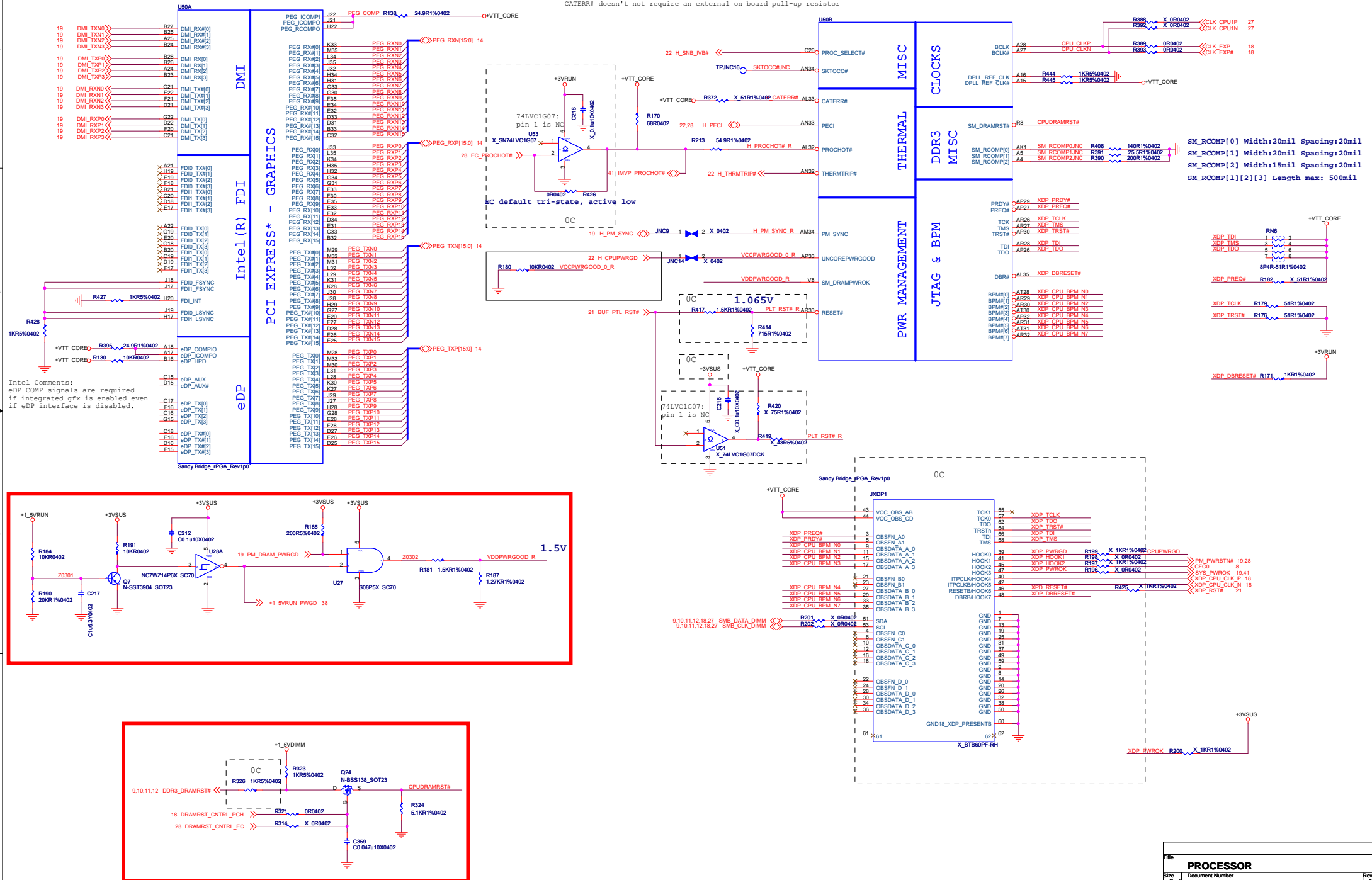
PCB Footprints



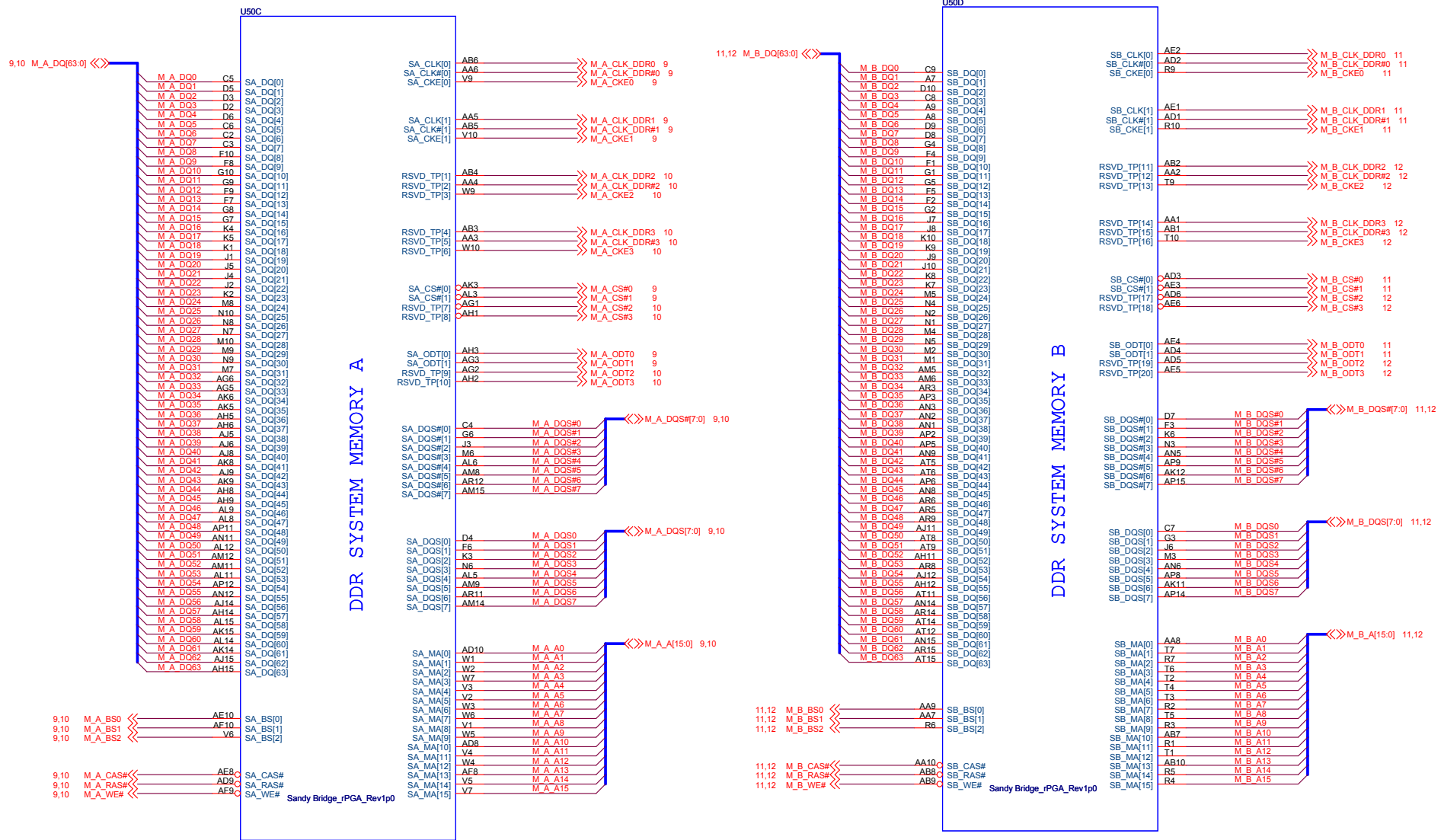
Power States	SLP S3#	SLP S4#	SLP S5#	+V*ALWAYS	+V*SUS	+V*RUN	CLK
S0 (Full on)	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft Off)	LOW	LOW	LOW	ON	OFF	OFF	OFF

**SANDYBRIDGE PROCESSOR (CLK,MISC,JTAG)**

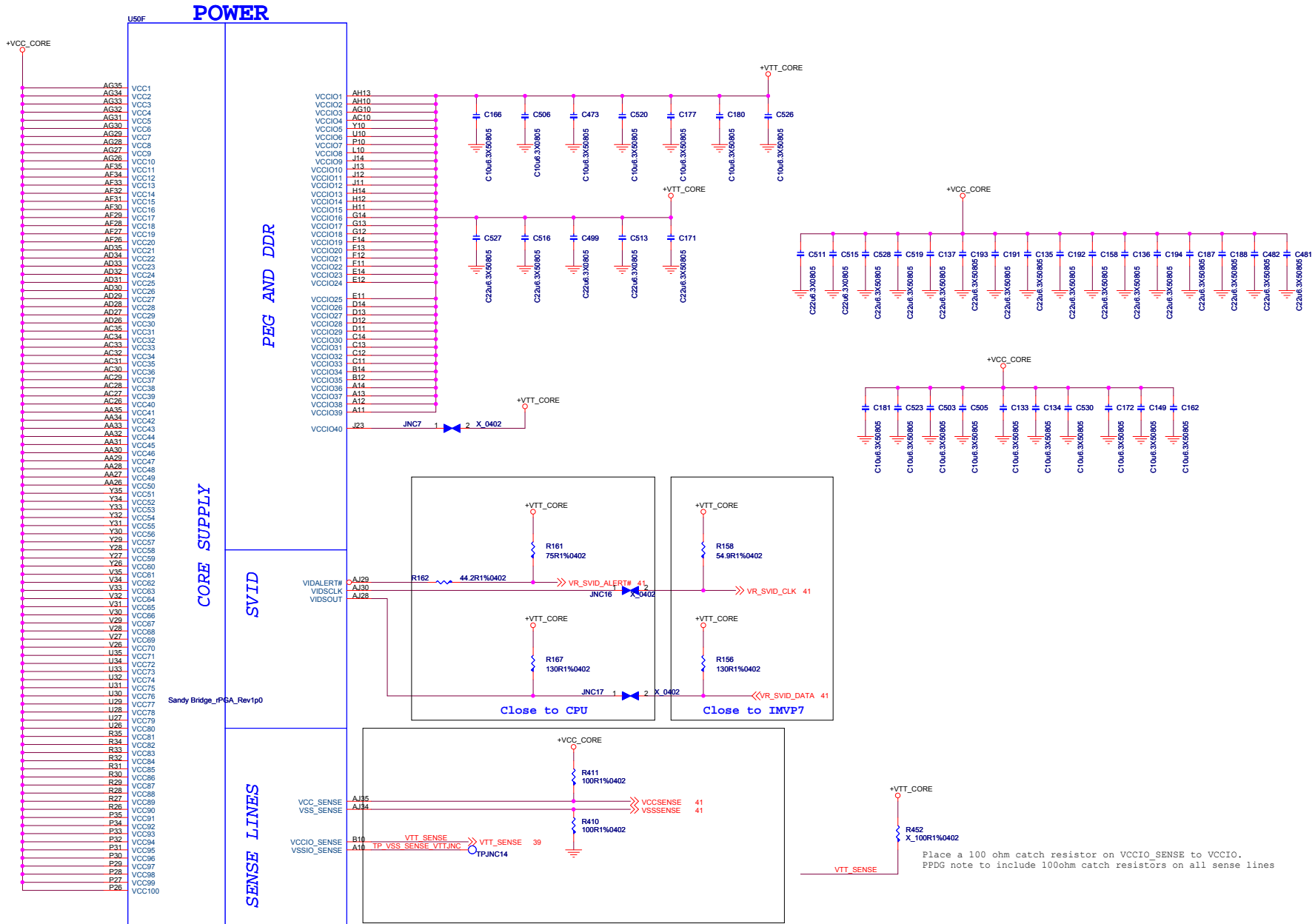
Intel Comments:  
CATERR# doesn't not require an external on board pull-up resistor



## SANDYBRIDGE PROCESSOR (DDR3)



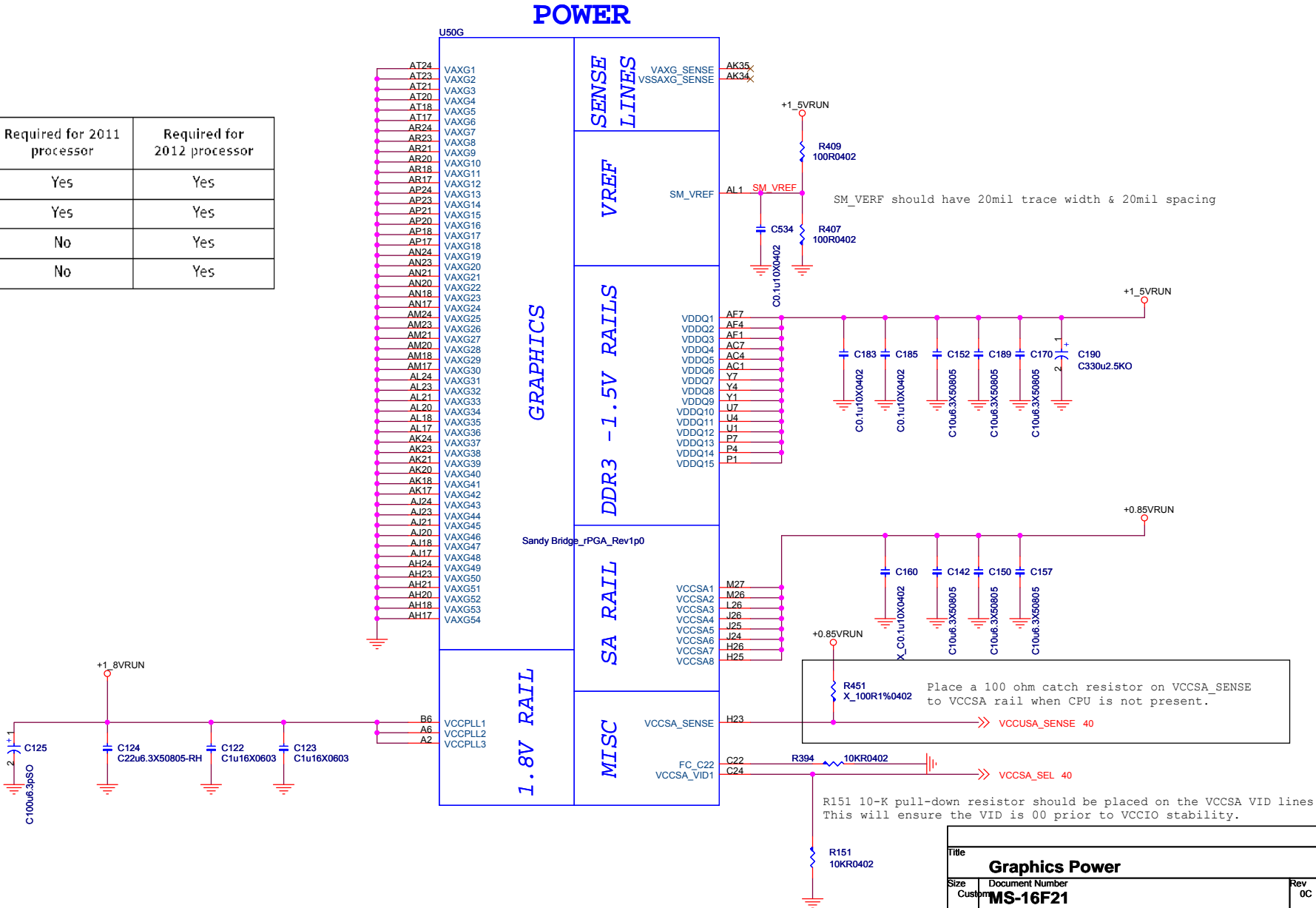
SANDYBRIDGE PROCESSOR (POWER)



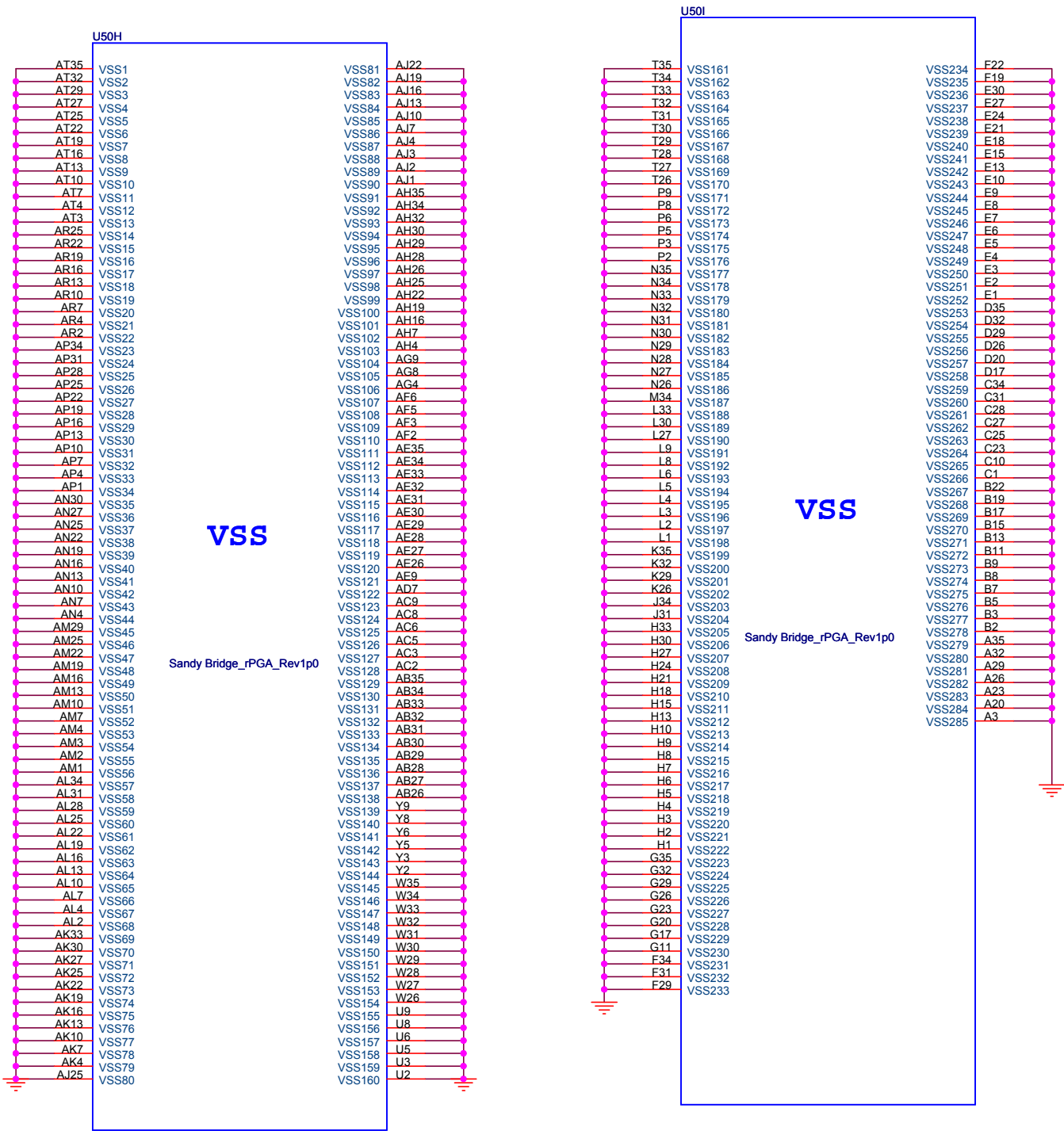
SANDYBRIDGE PROCESSOR (GRAPHICS POWER)

VCCSA\_SEL Voltage Selection Table

VID[0] Pin C22	VID[1] Pin C24	VCCSA Vout	Required for 2011 processor	Required for 2012 processor
0	0	0.90 V	Yes	Yes
0	1	0.80 V	Yes	Yes
1	0	0.725 V	No	Yes
1	1	0.675 V	No	Yes

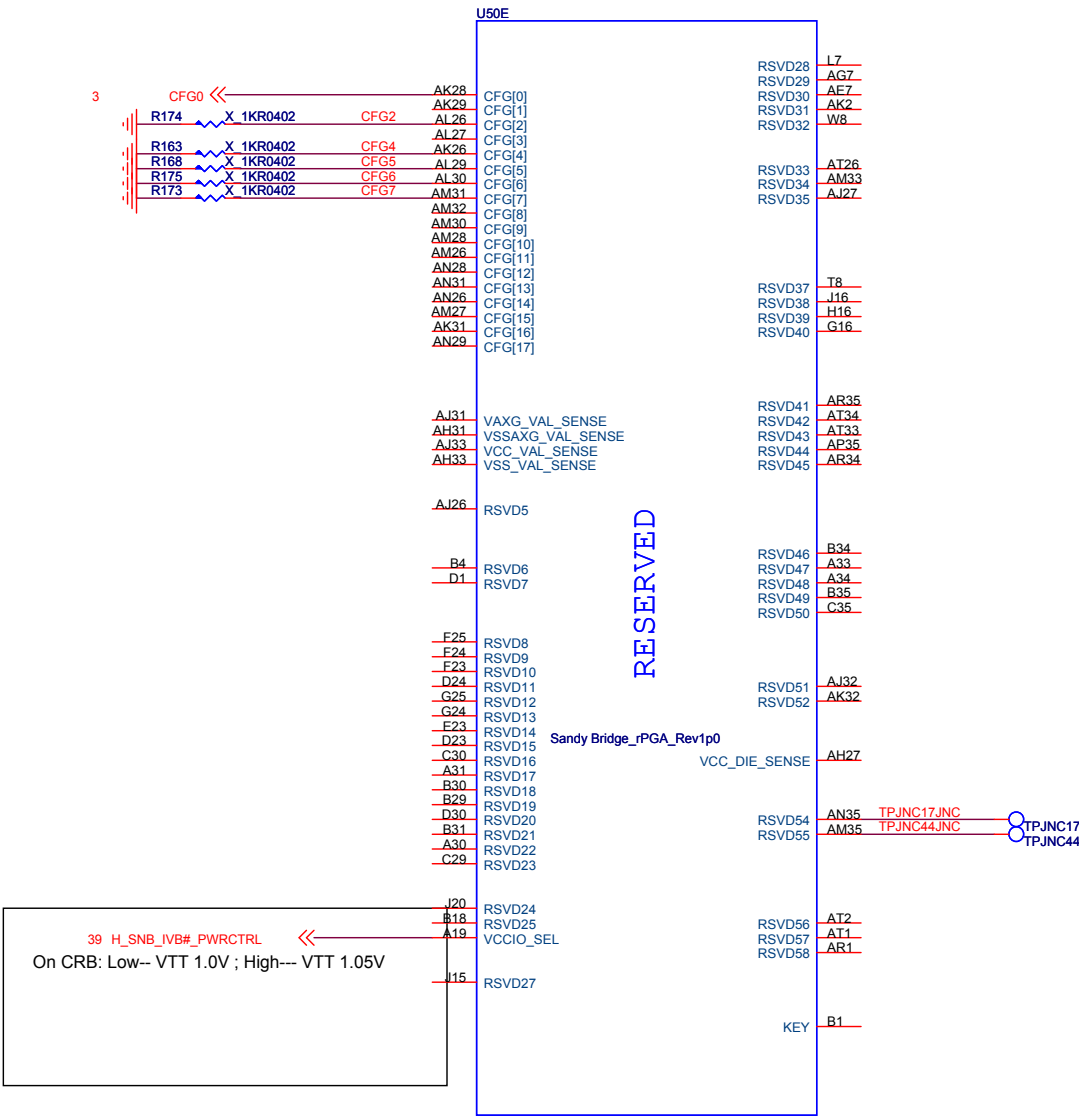


SANDYBRIDGE PROCESSOR (GND)



Title			
PROCESSOR GND			
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Custom	MS-16F21		
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SANDYBRIDGE PROCESSOR (RESERVED)



CFG3 - PCI-Express Static Lane Reversal	
CFG2	1 :Normal Operation 0 :Lane Numbers Reversed 15 -> 0, 14 -> 1, ...

CFG4 - Display Port Presence	
CFG4	1:Disabled; No Physical Display Port attached to Embedded Display Port  0:Enabled; An external Display Port device is connected to the Embedded Display Port

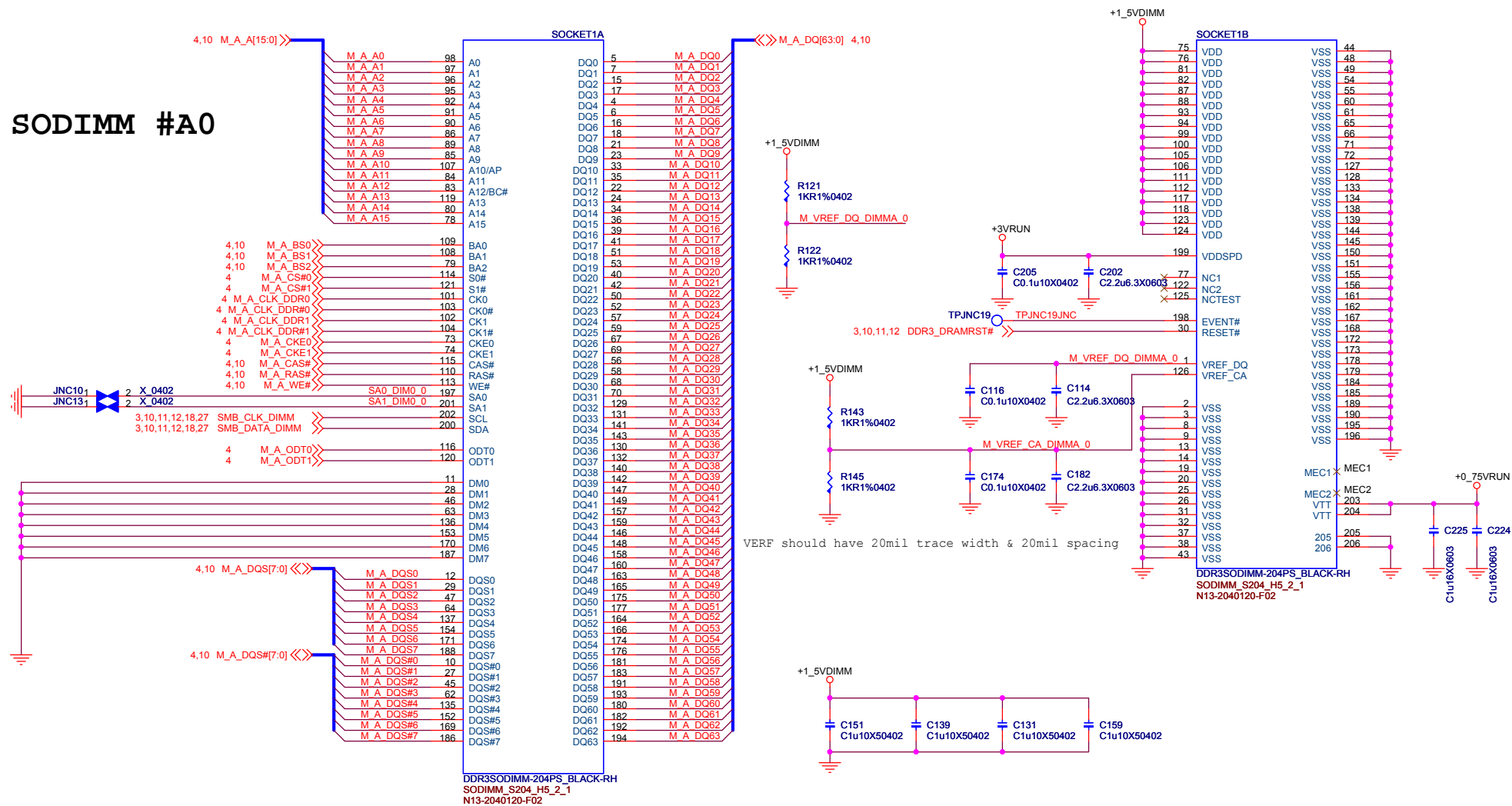
PCI-Express Configuration Select	
CFG[5:6]	11:Default X16-device 1 functions 1 and 2 disabled 10: X8 X8-device 1 functions 1 enable, function2 disabled  01:Reserved--(device 1 functions 1disabled function2 enable 00: X8 X4 X4-device 1 functions 1 and 2 enable

PEG DEFER TRAINING	
CFG7	1 : (Default)PEG train immediately following xxRESETB de assertion 0 :PEG wait for BIOS for training

Title		
PROCESSOR RESERVED		
Size	Document Number	Rev
Custom	MS-16F21	0C
Date:	Wednesday, June 30, 2010	Sheet 8 of 57

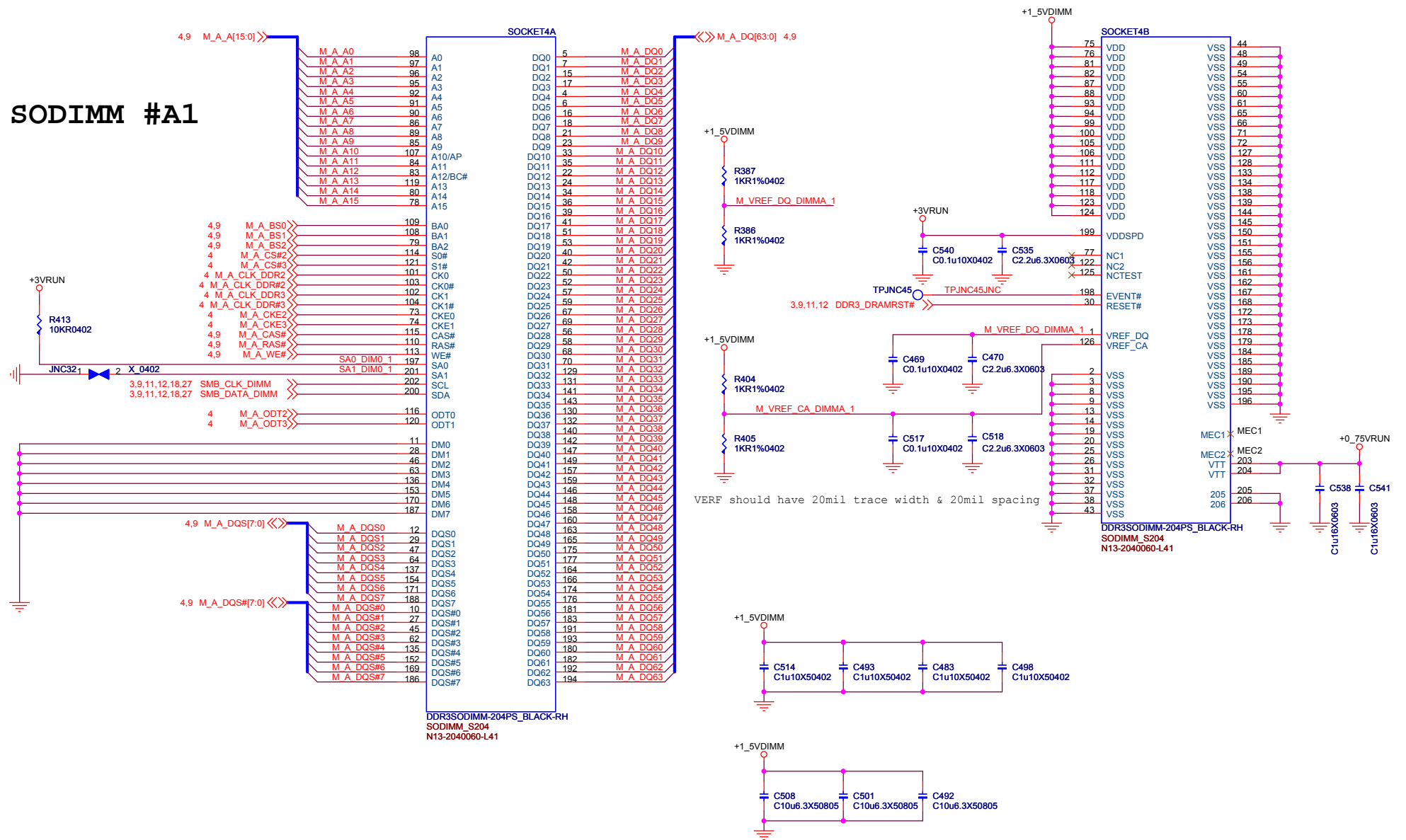


## SODIMM #A0



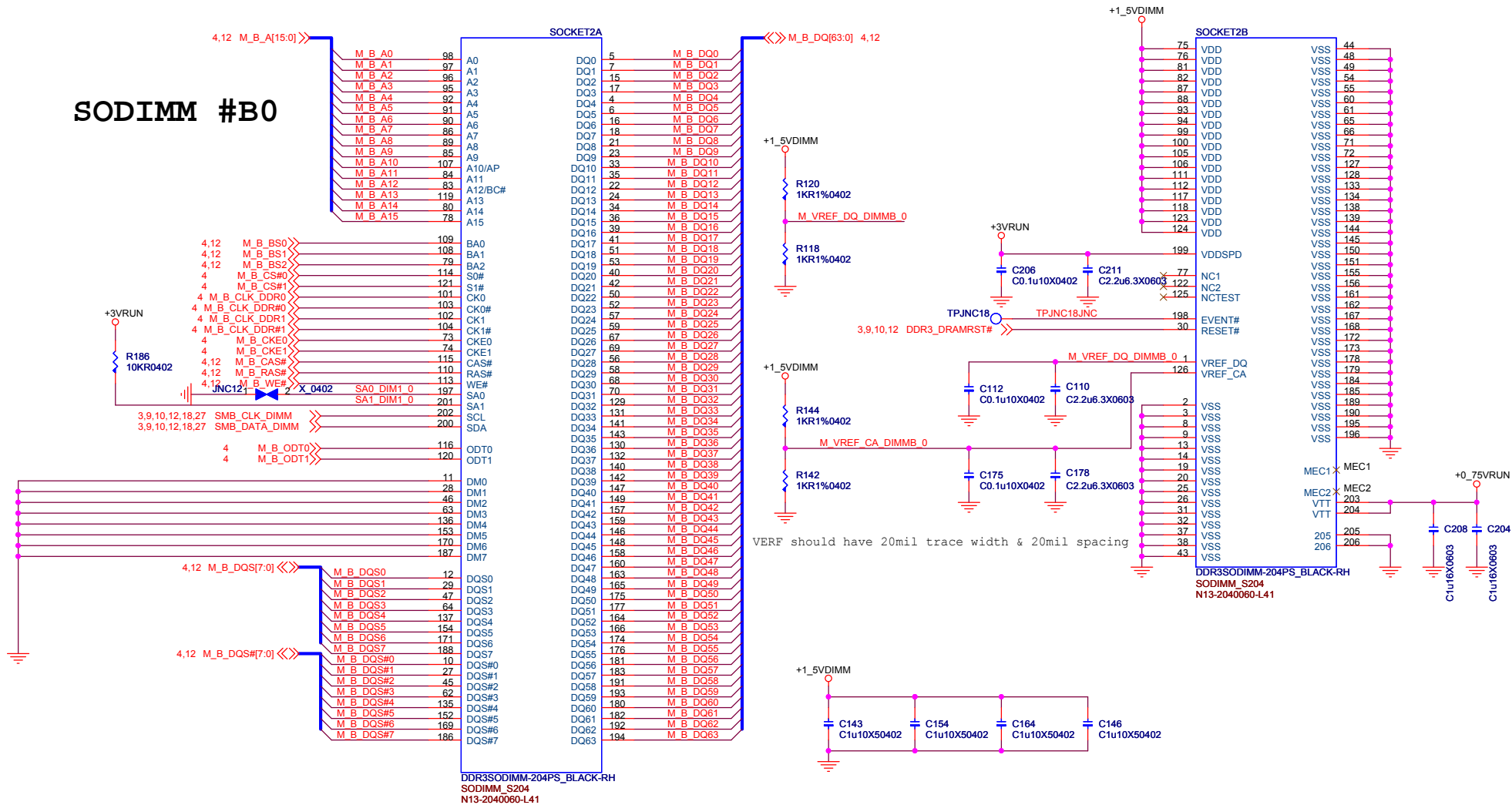
Title				
DDR3 SODIMM A0				
Size	Document Number			Rev
Customer	MS-16F21			OC
Date:	Wednesday, June 30, 2010	Sheet	9	of 57

**SODIMM #A1**



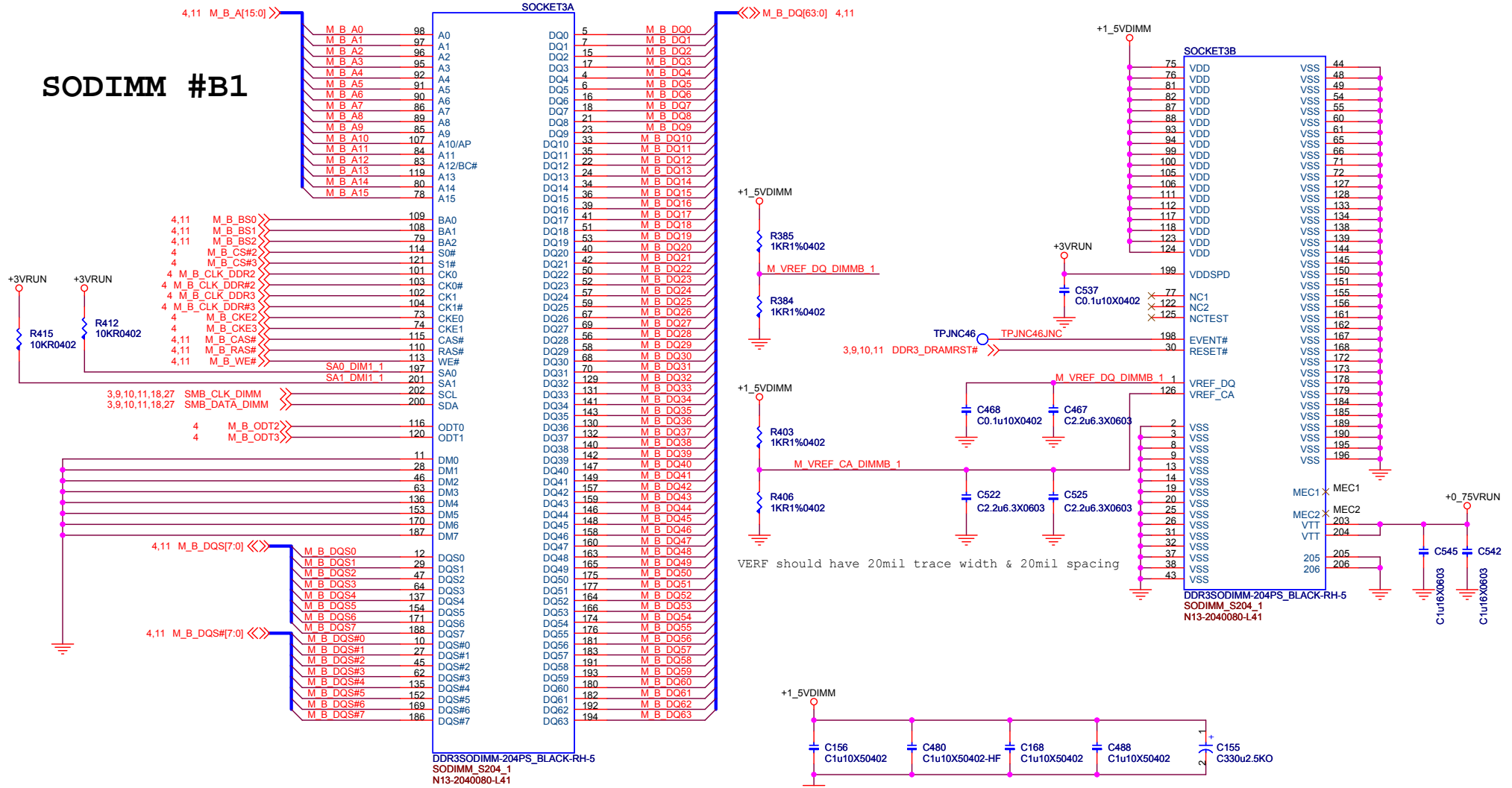
Title				
DDR3 SODIMM A1				
Size	Document Number			Rev
Custom	MS-16F21			OC
Date:	Wednesday, June 30, 2010	Sheet	10 of 57	

# SODIMM #B0

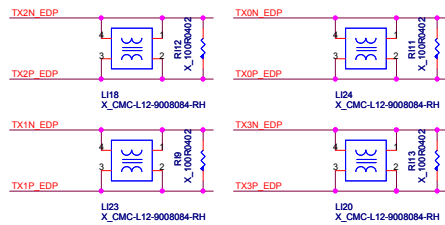
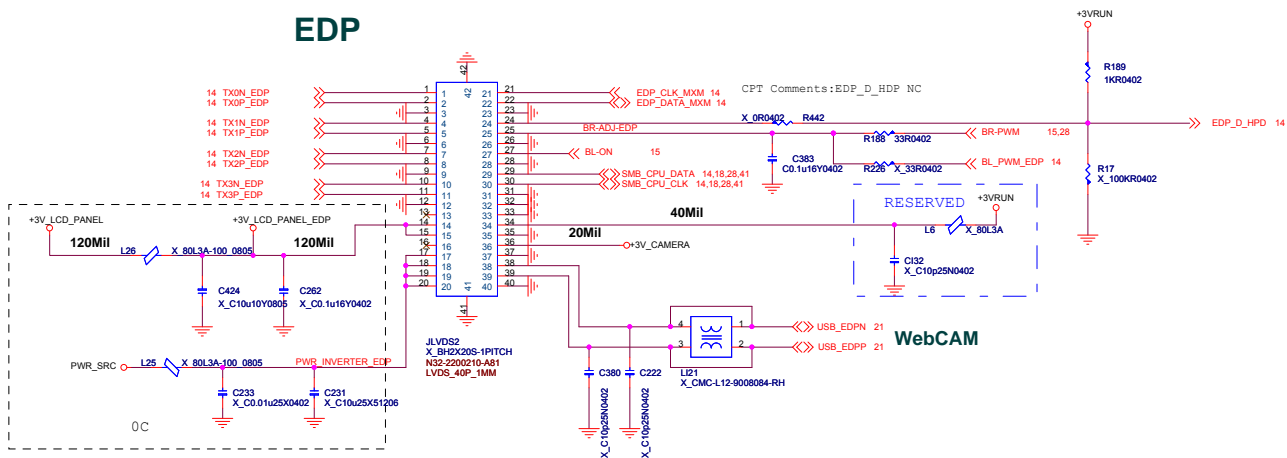


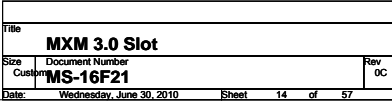
Title				
DDR3 SODIMM B0				
Size	Document Number			Rev
Custom	MS-16F21			0C
Date:	Wednesday, June 30, 2010	Sheet	11 of 57	

# SODIMM #B1

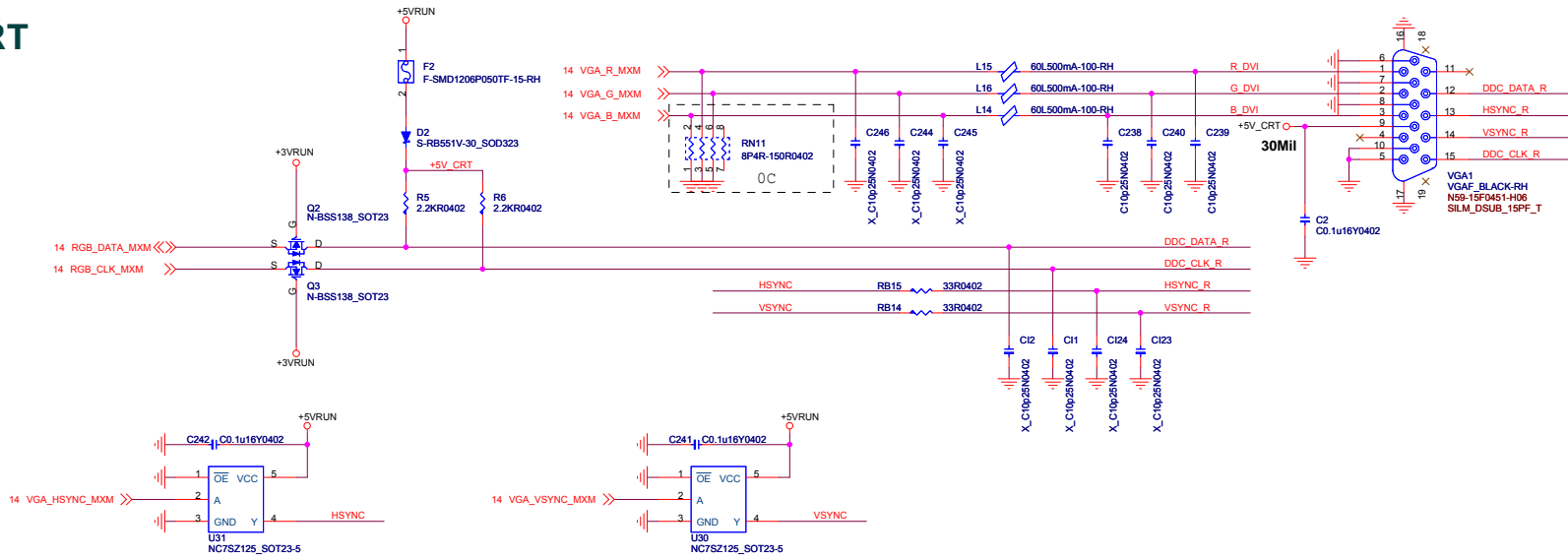


# EDP

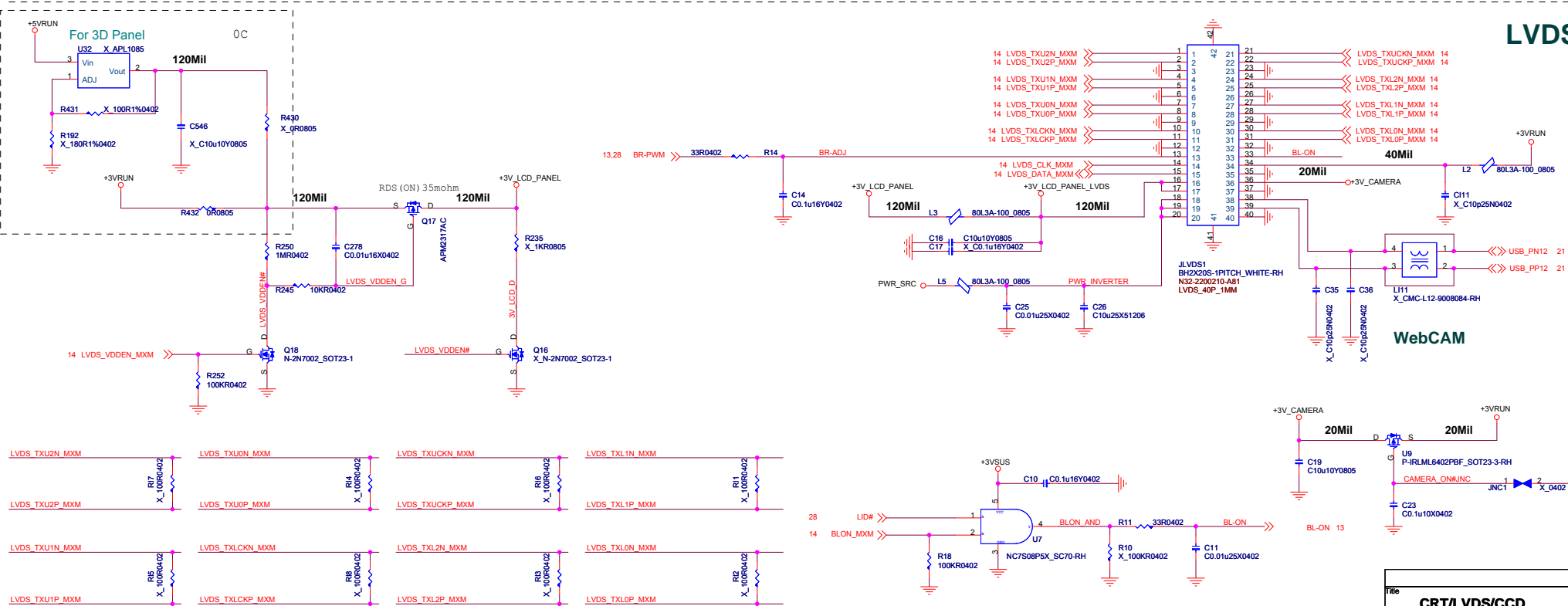




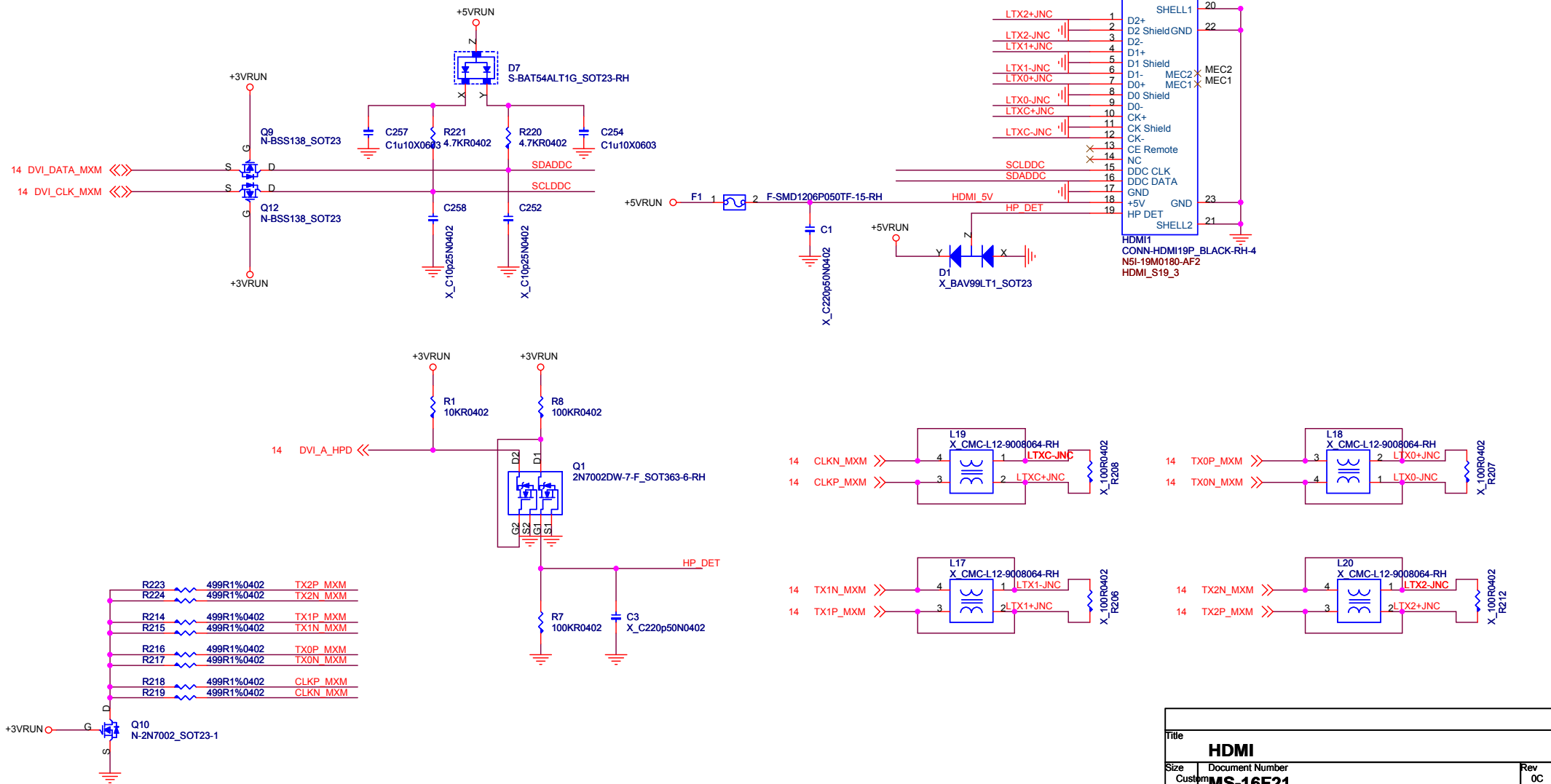
# CRT



# LVDS



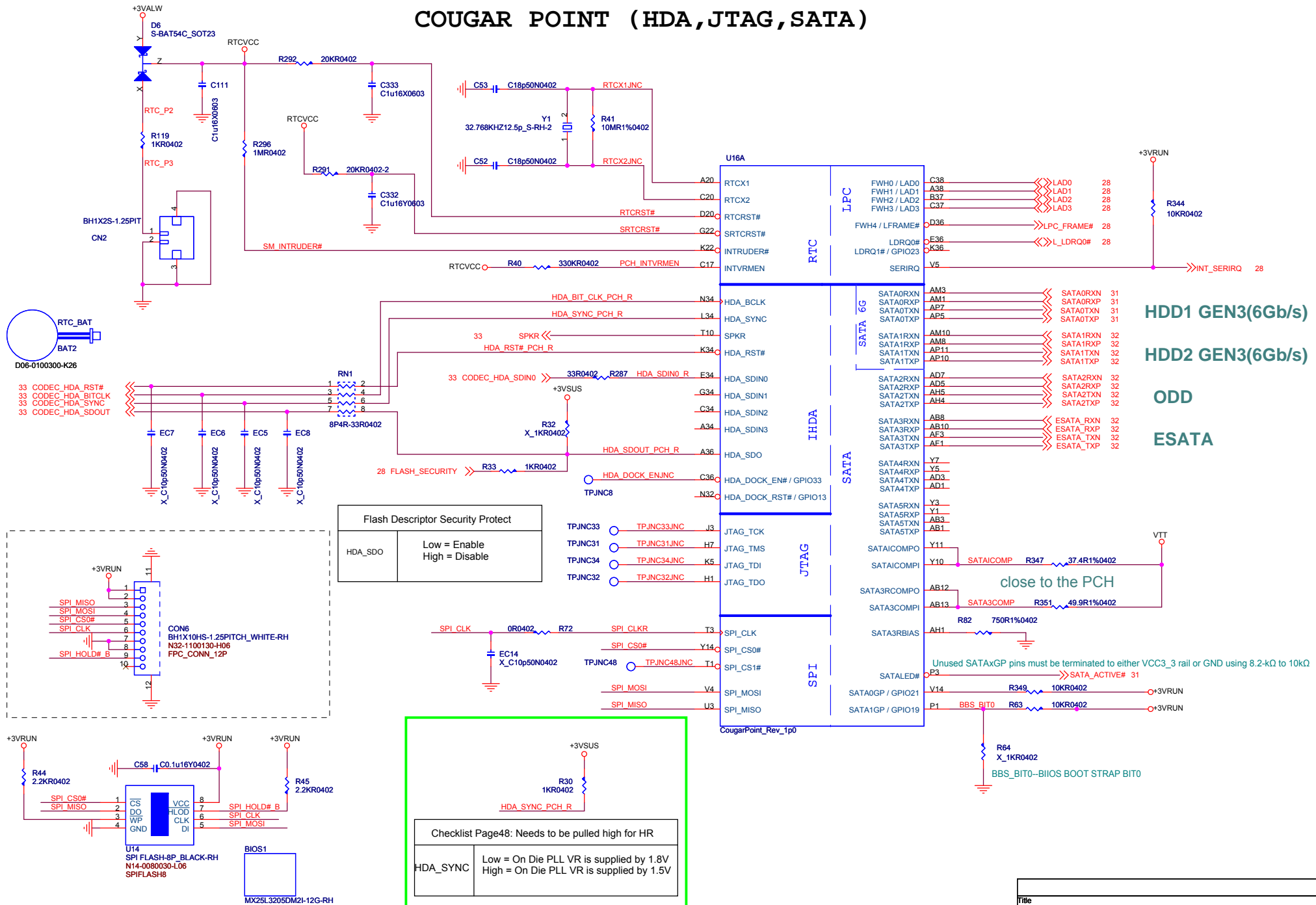
Title		
CRT/LVDS/CCD		
Size	Document Number	Rev
Custom	MS-16F21	OC
Date:	Tuesday, June 29, 2010	Sheet 15 of 57



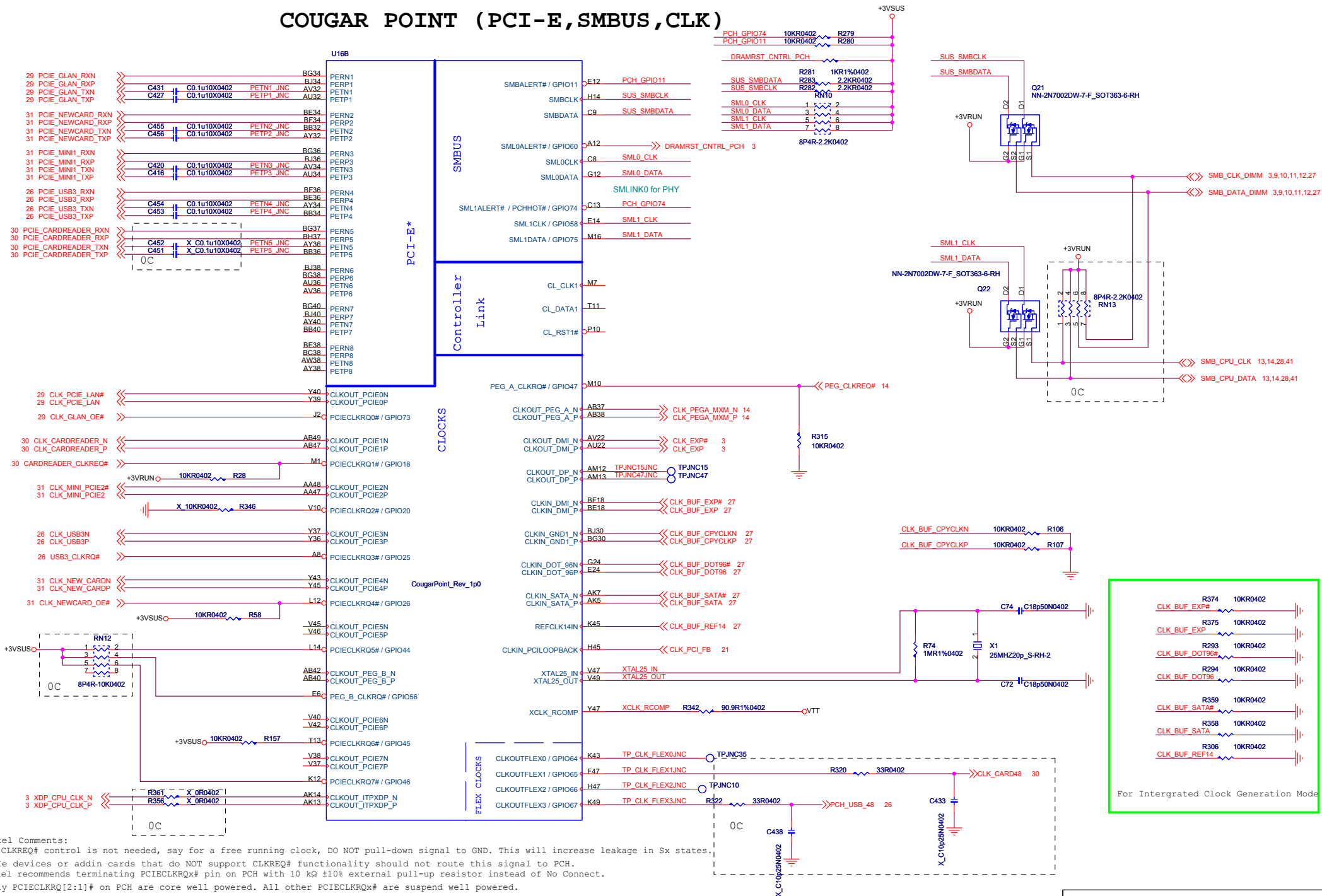
Title		
HDMI		
Size	Document Number	Rev
Custom	MS-16F21	0C
Date:	Tuesday, June 29, 2010	Sheet 16 of 57



# COUGAR POINT (HDA,JTAG,SATA)

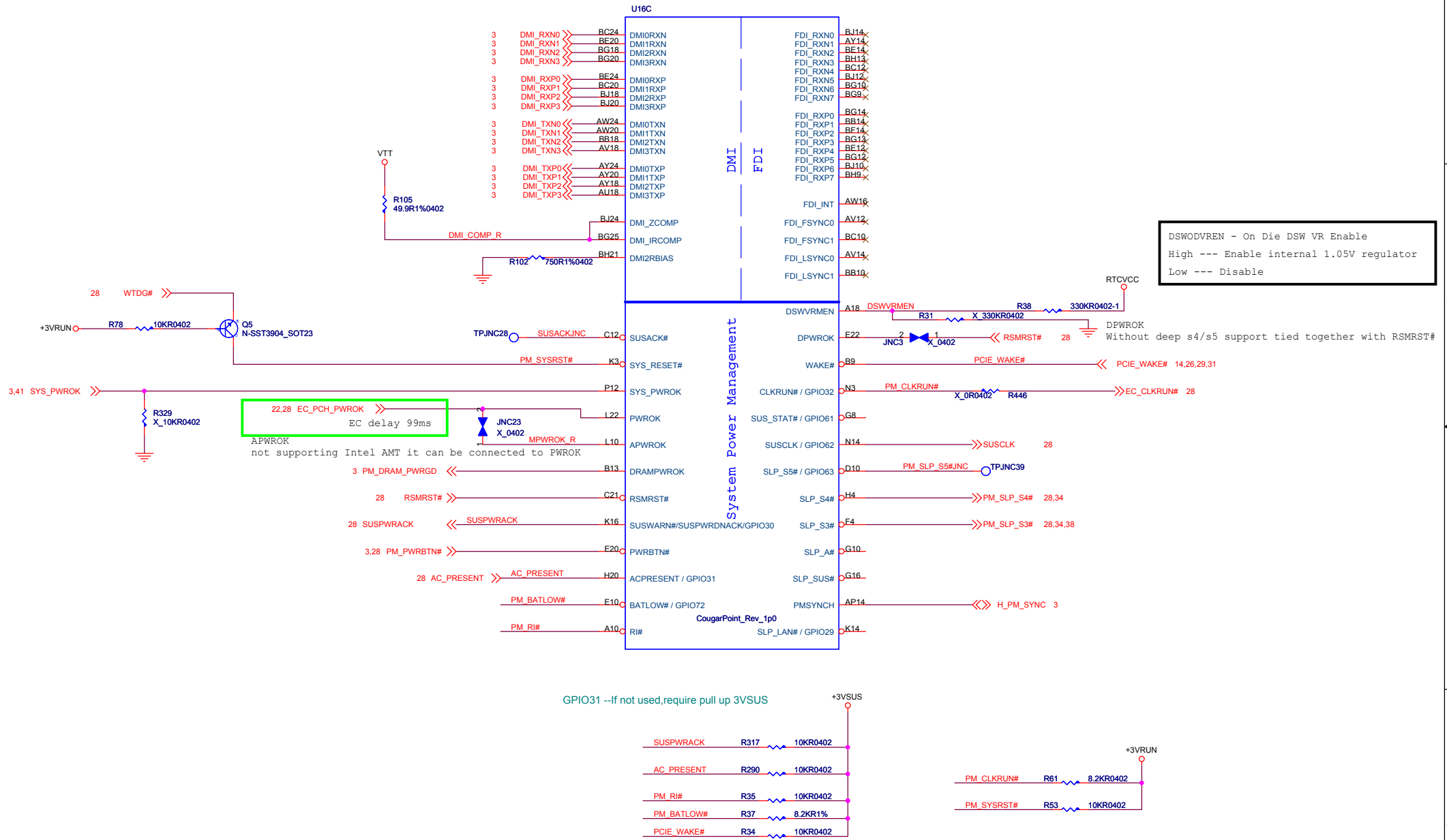


# COUGAR POINT (PCI-E, SMBUS, CLK)



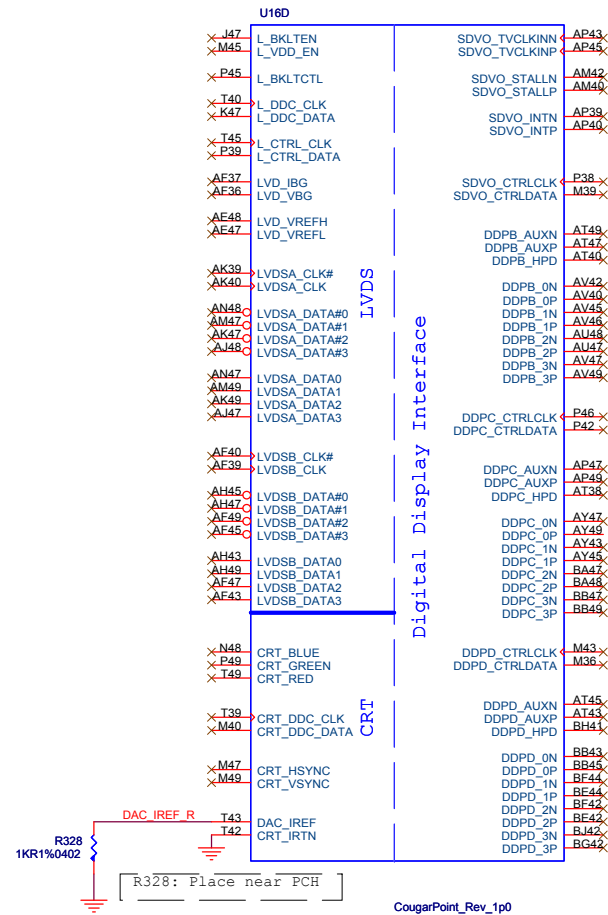
Title			<b>PCH_PCIE/SMBUS/CLK</b>
Size	Document Number	Rev	
Custom	<b>MS-16F21</b>	0C	
Date:	Thursday, July 01, 2010	Sheet	18 of 57

# COUGAR POINT (DMI, FDI, GPIO)

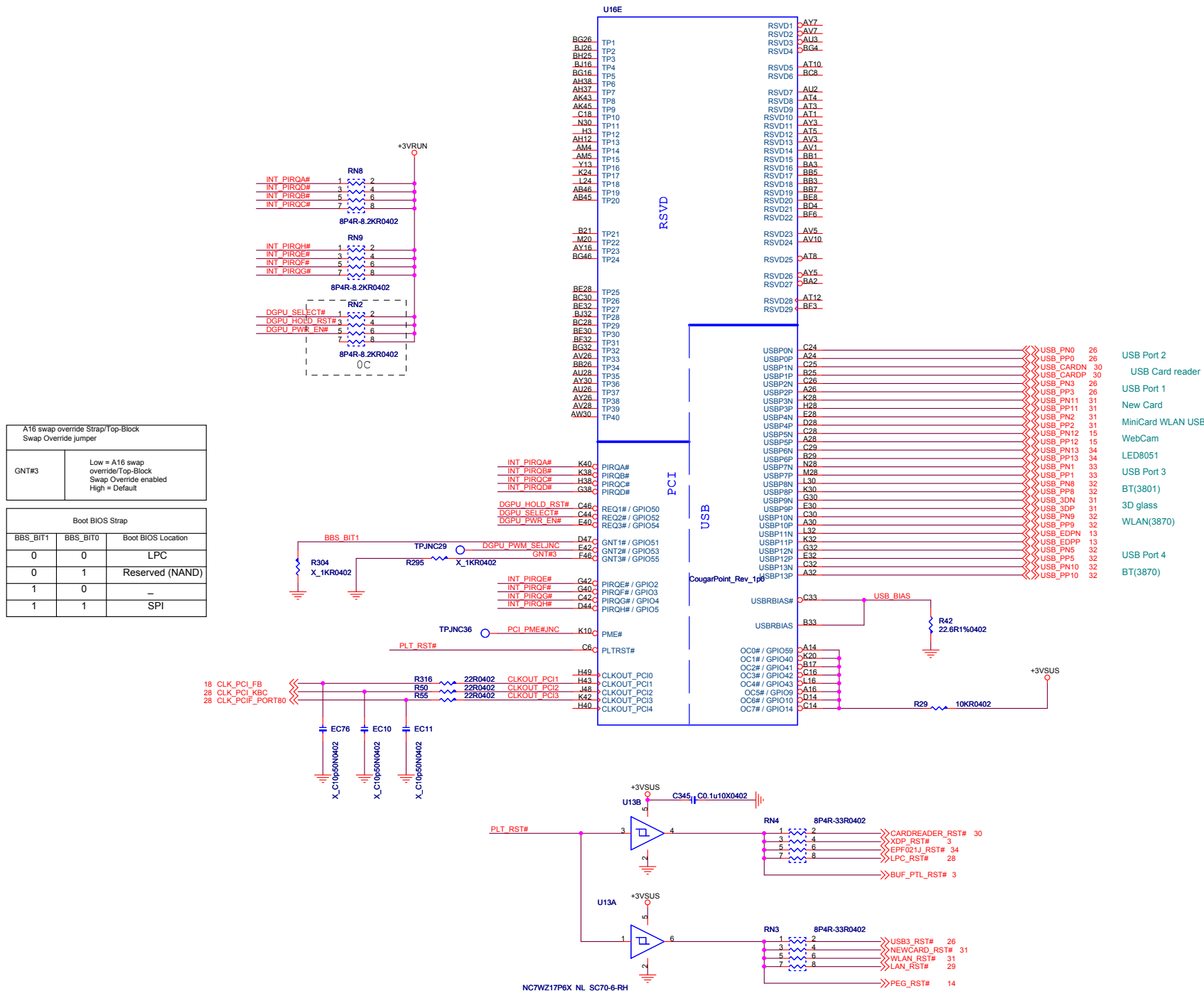


DSWVRMEN - On Die DSW VR Enable  
High --- Enable internal 1.05V regulator  
Low --- Disable

# COUGAR POINT (LVDS,DDI)



# COUGAR POINT (PCI,USB,NVRAM)



GPIO0 & 6 & 16 & 17 & 22 & 34 & 38 & 48 --If not used,require pull up 3VRUN  
GPIO57 --If not used,require pull up 3VSUS  
GPIO15--Not support AMT,Transport Layer Security Disable(High is support TLS,internal pull-down)  
GPIO27 is deep S4 & S5 weak up event,internal pull high.& It's VCCFDIPLL internal VRM strapping pin  
GPIO35 --Define to EDID Select (If not used,require pull down)

## COUGAR POINT (GPIO,VSS\_NCTF,RSVD)

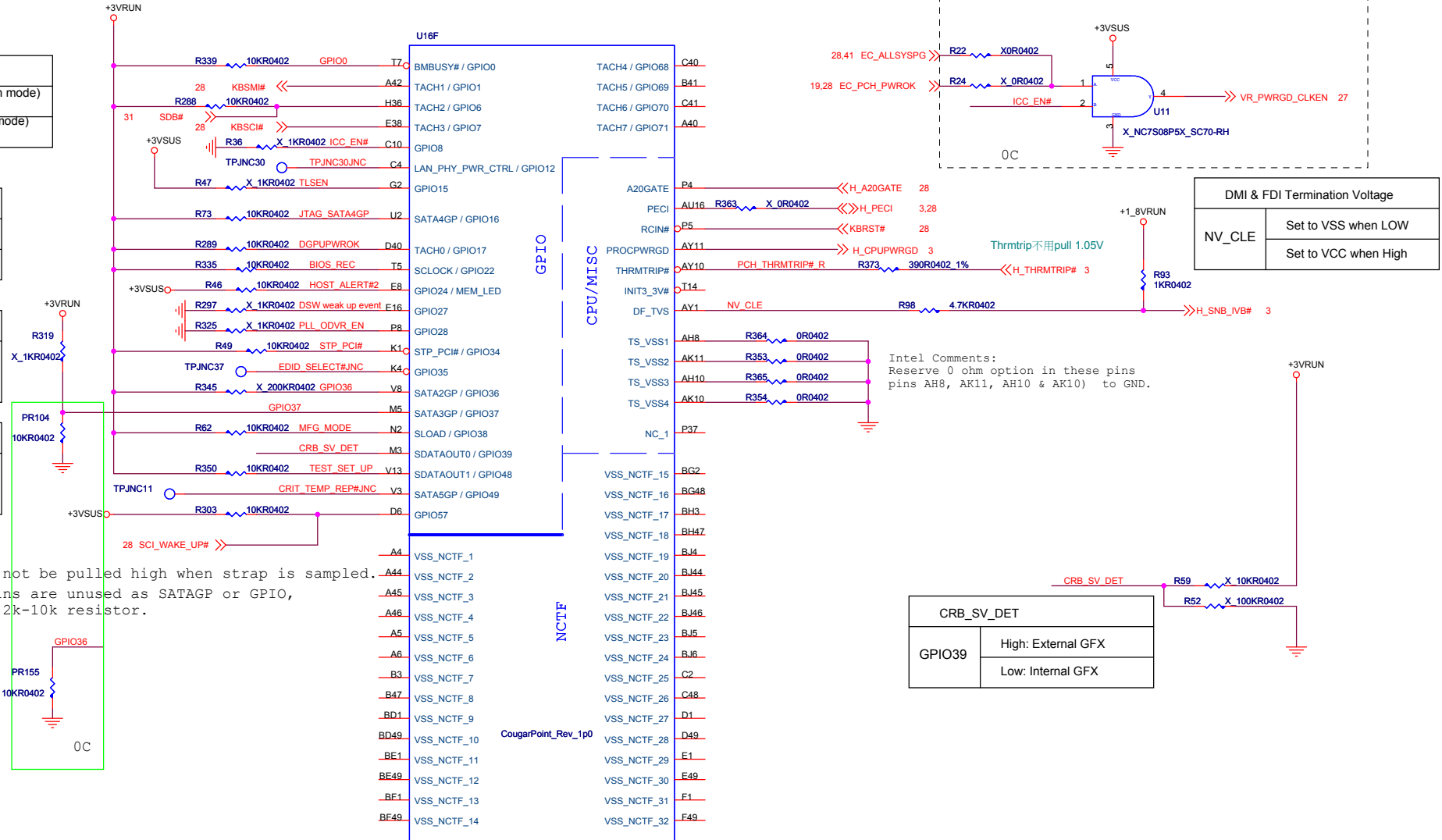
Integrated Clock Chip Enable	
ICC_EN	High: use CK505 (buffer through mode) internal pull high
	Low: use PCH( integrated clock mode)

PLL ON DIE VR_ENABLE	
GPIO28	Internal pull high (Enable)
	Low: Disable

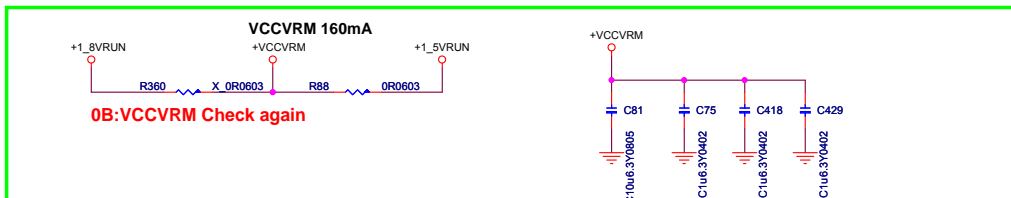
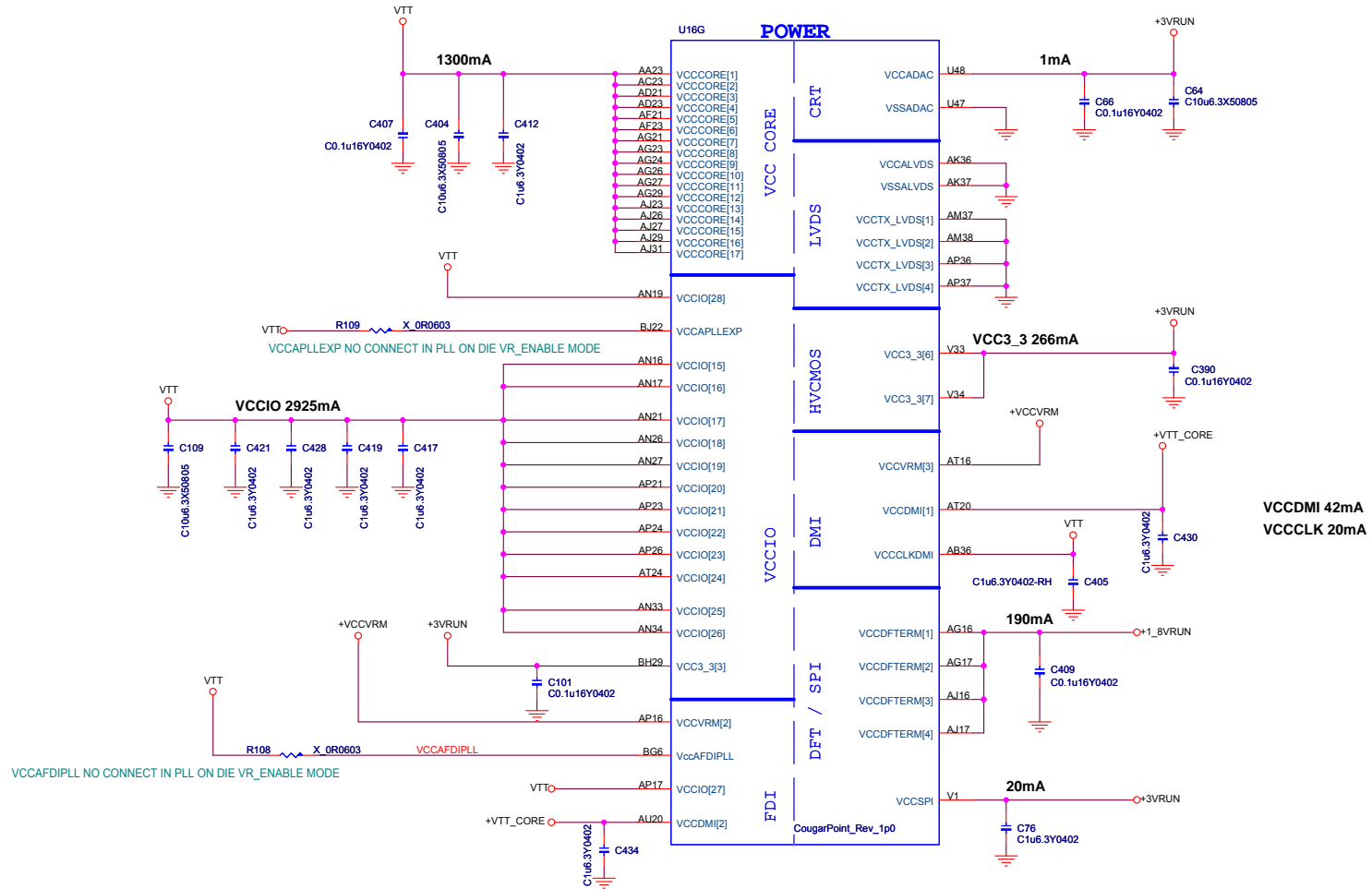
DMI termination voltage override	
GPIO36	Low-- TX,RX terminated to same voltage (DC coupling mode)default
	High: TX,RX terminated to same voltage (DC coupling mode)default

FDI termination voltage override	
GPIO37	Low-- TX,RX terminated to same voltage (DC coupling mode)default
	High: TX,RX terminated to same voltage (DC coupling mode)default

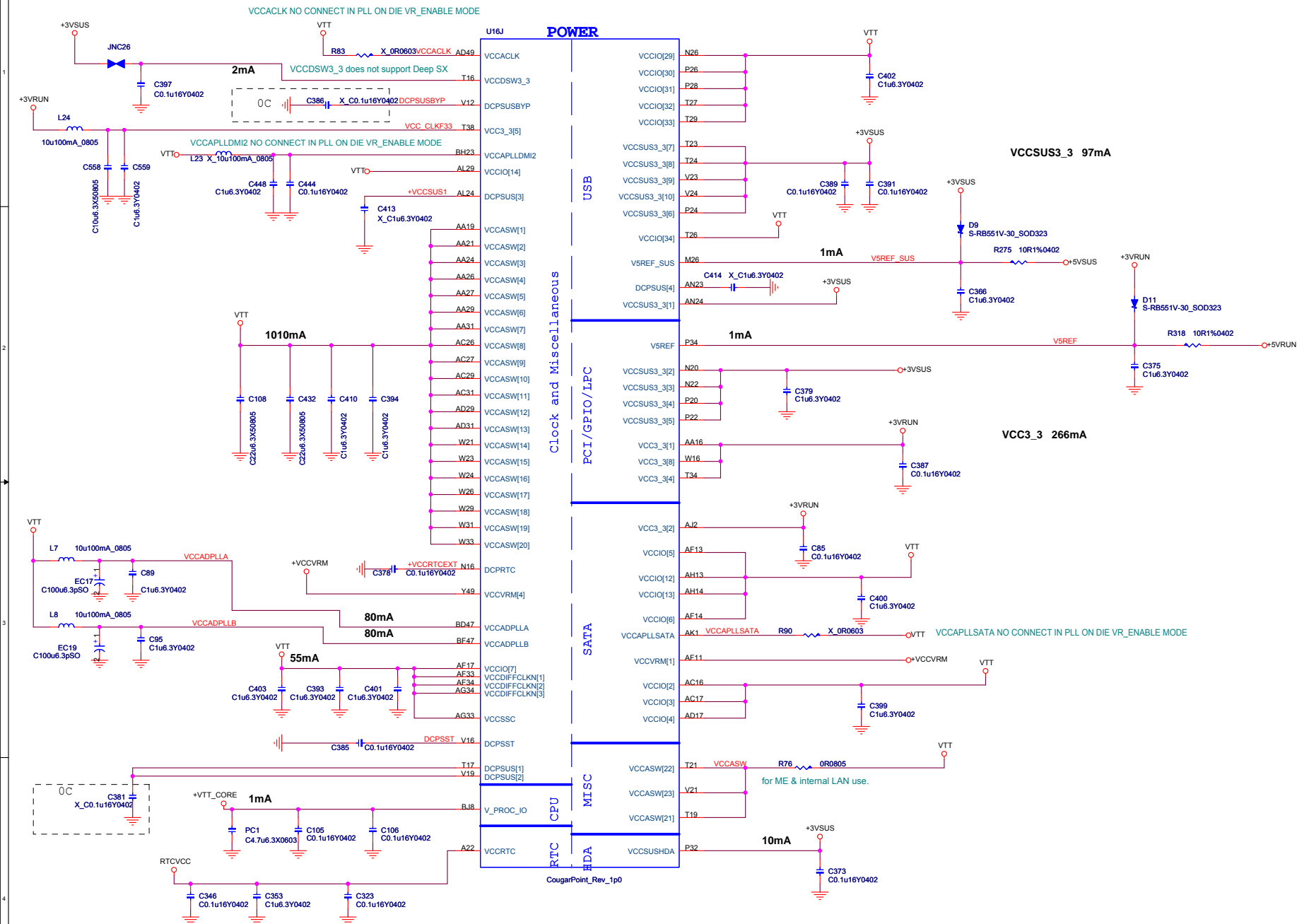
PCH EDS1.0:GP1036&37 should not be pulled high when strap is sampled.  
PCH EDS1.1:GP1036&37 when pins are unused as SATAGP or GPIO,  
terminate them to VSS via 8.2k-10k resistor.



## COUGAR POINT (POWER)

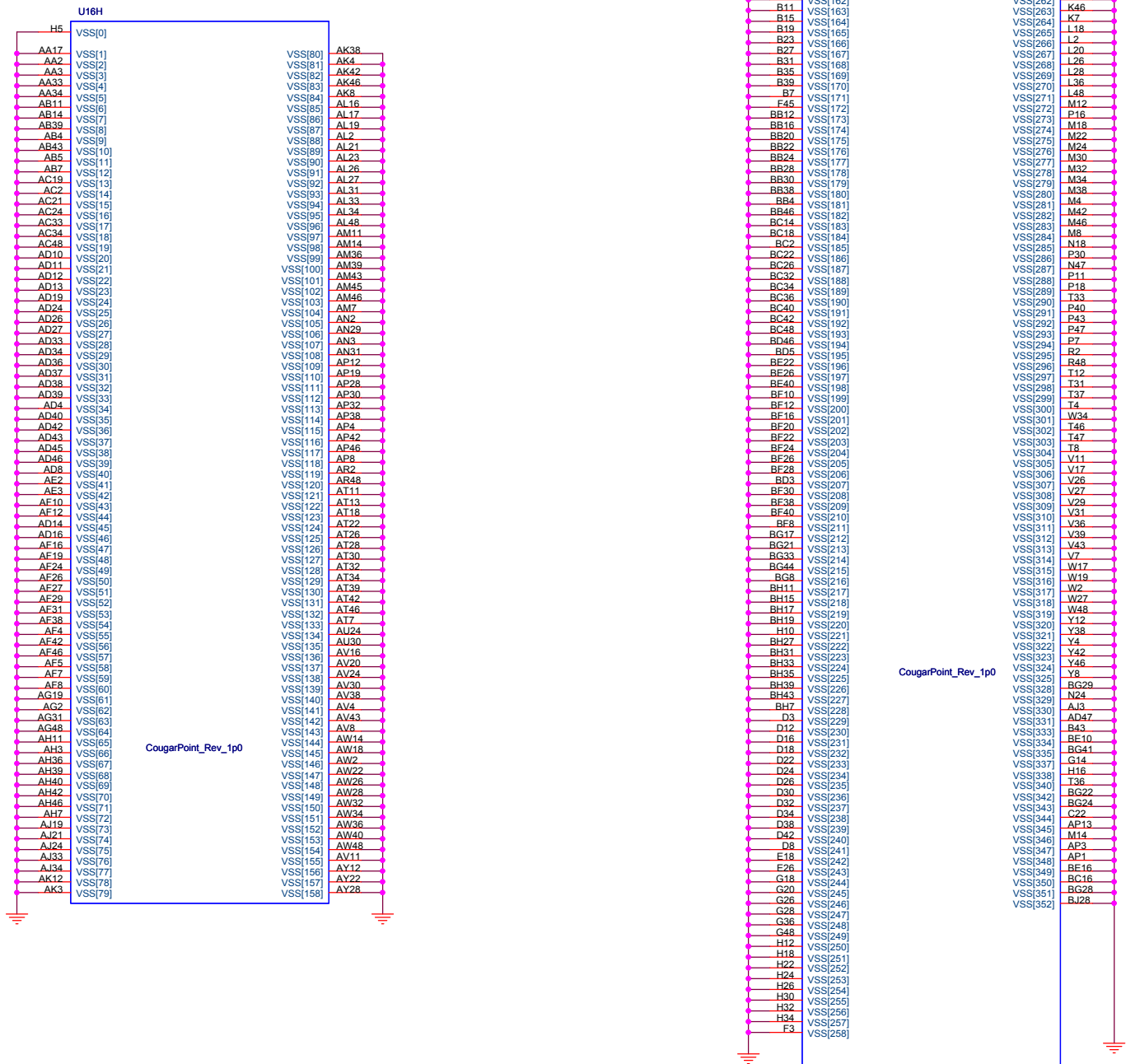


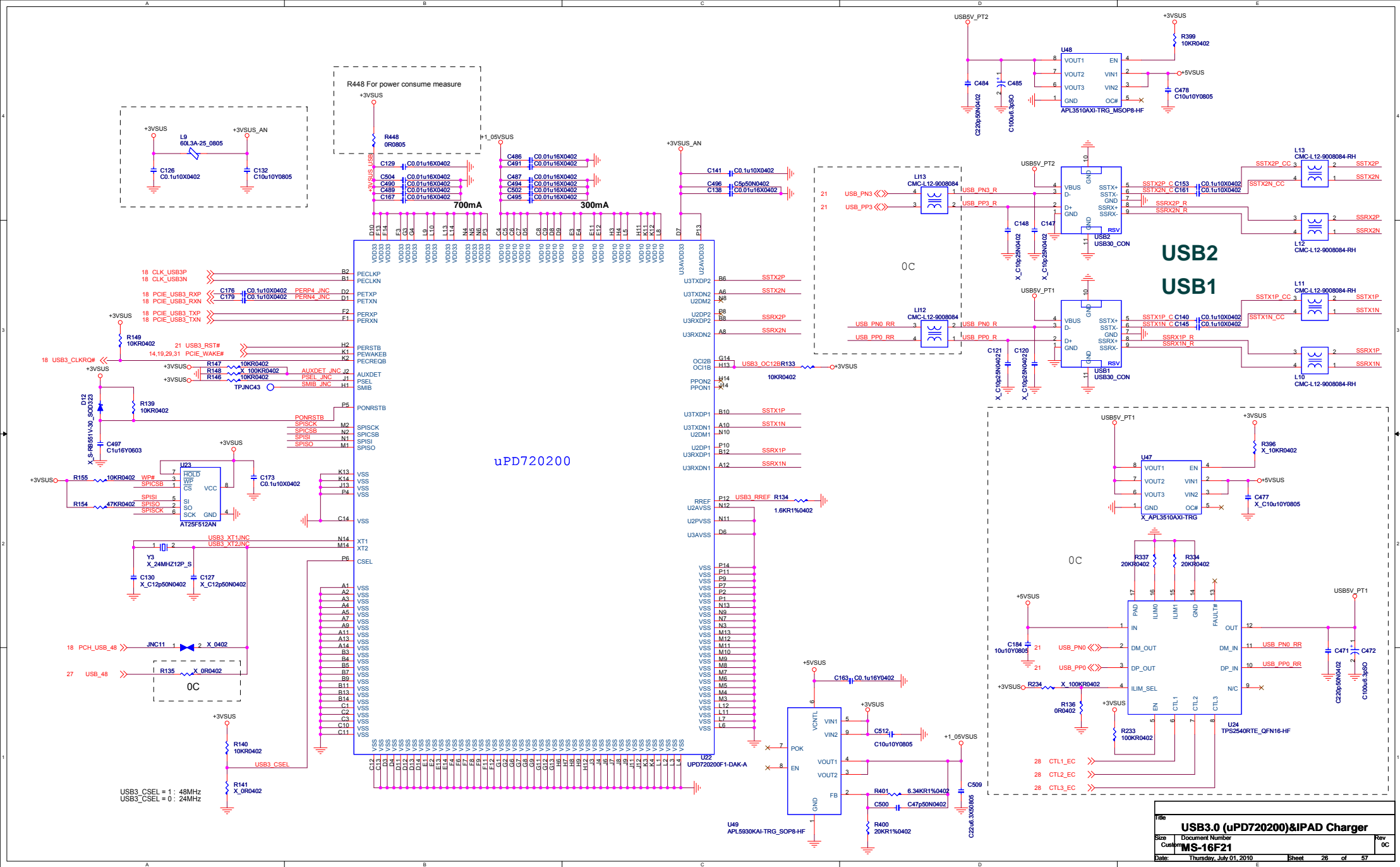
## COUGAR POINT (POWER)

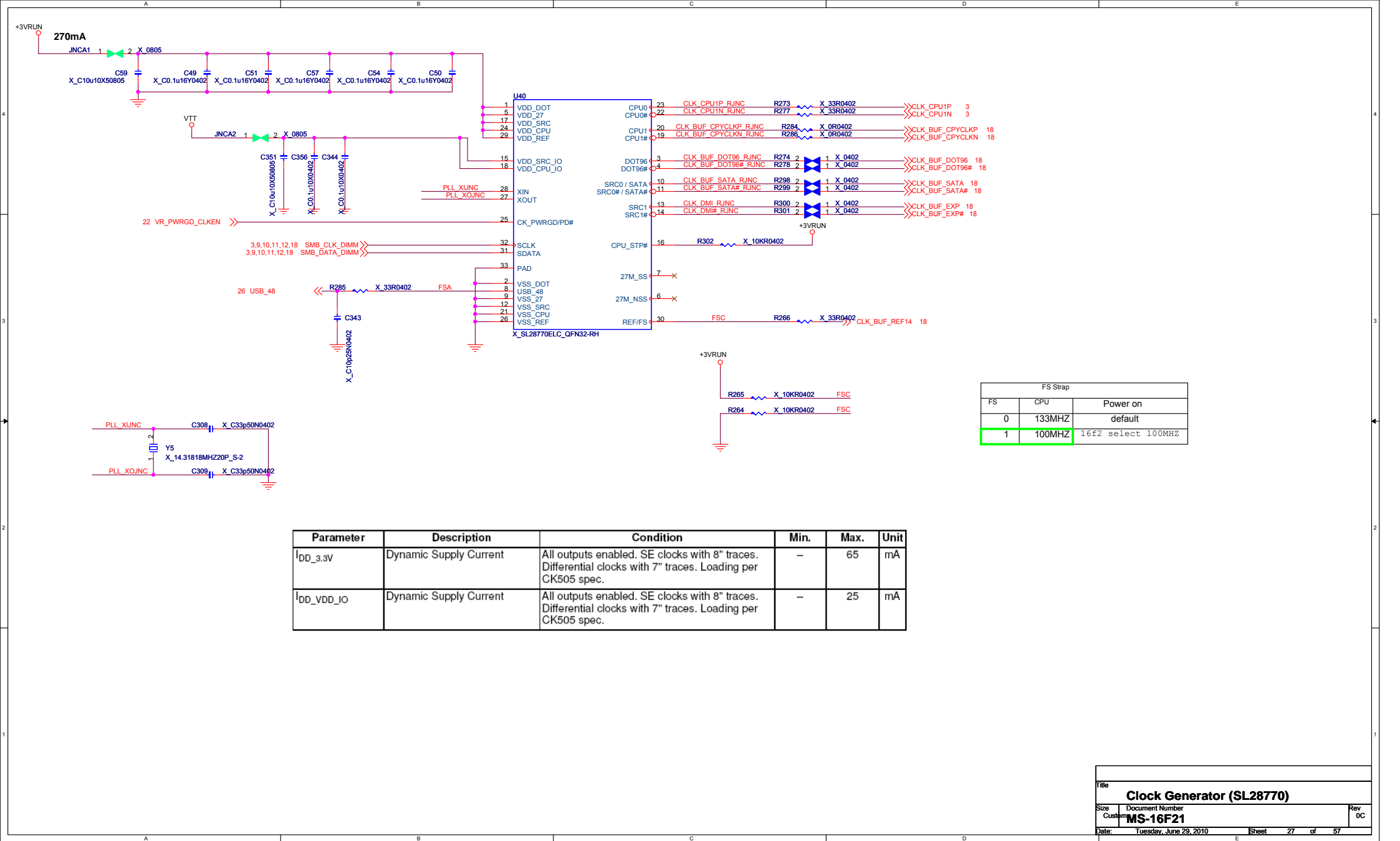


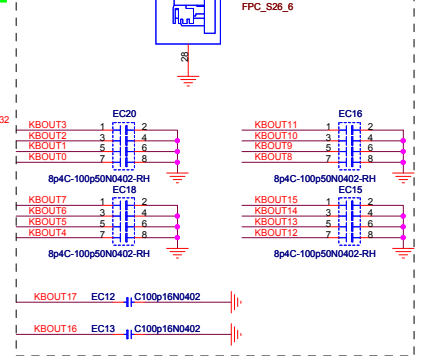
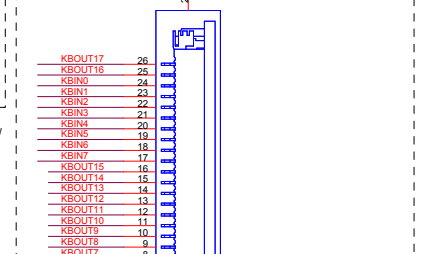


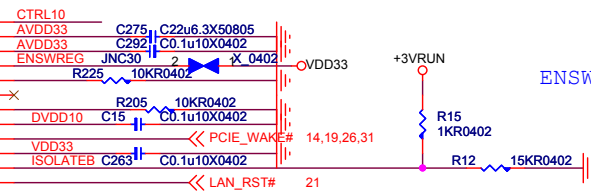
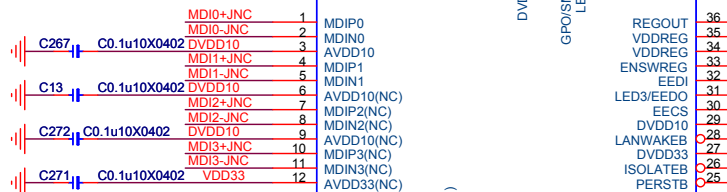
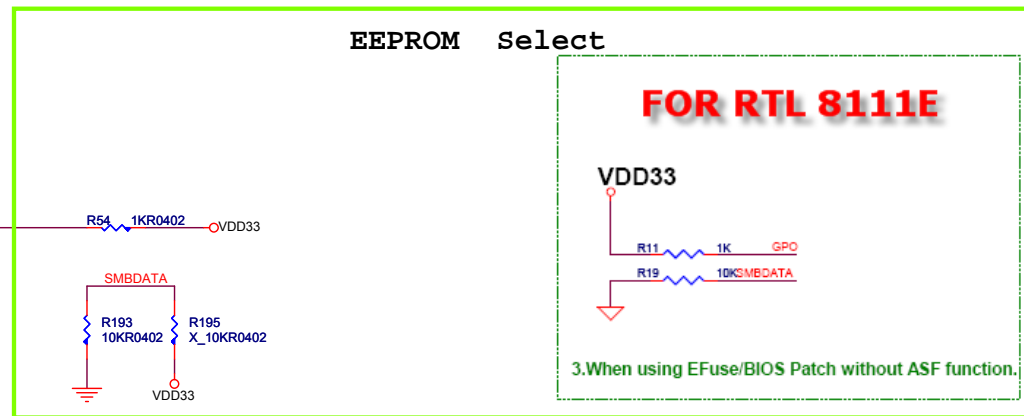
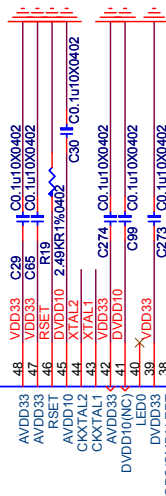
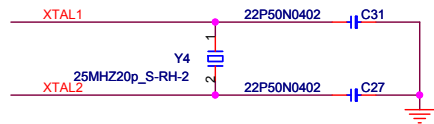
Cougar Point (GND)



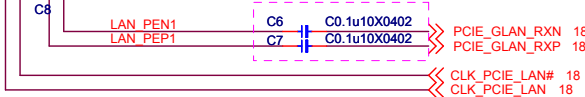
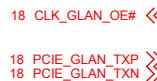
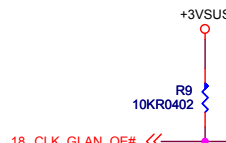
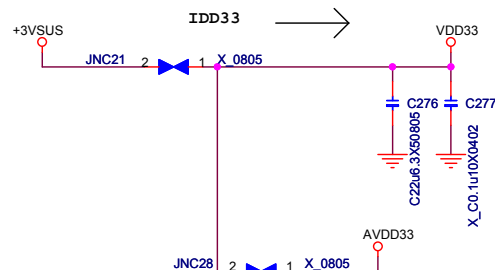
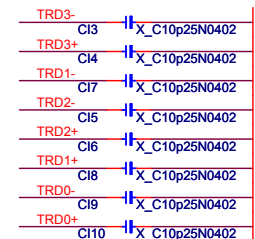




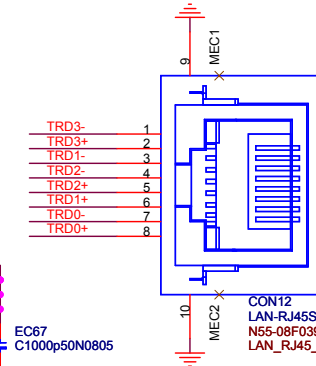
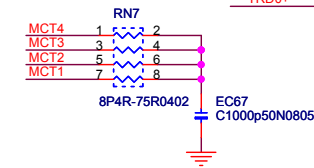
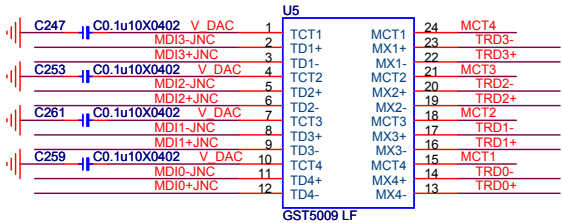




ENSWREG: ENABLE SWITCH LDO



### Transfer Mode

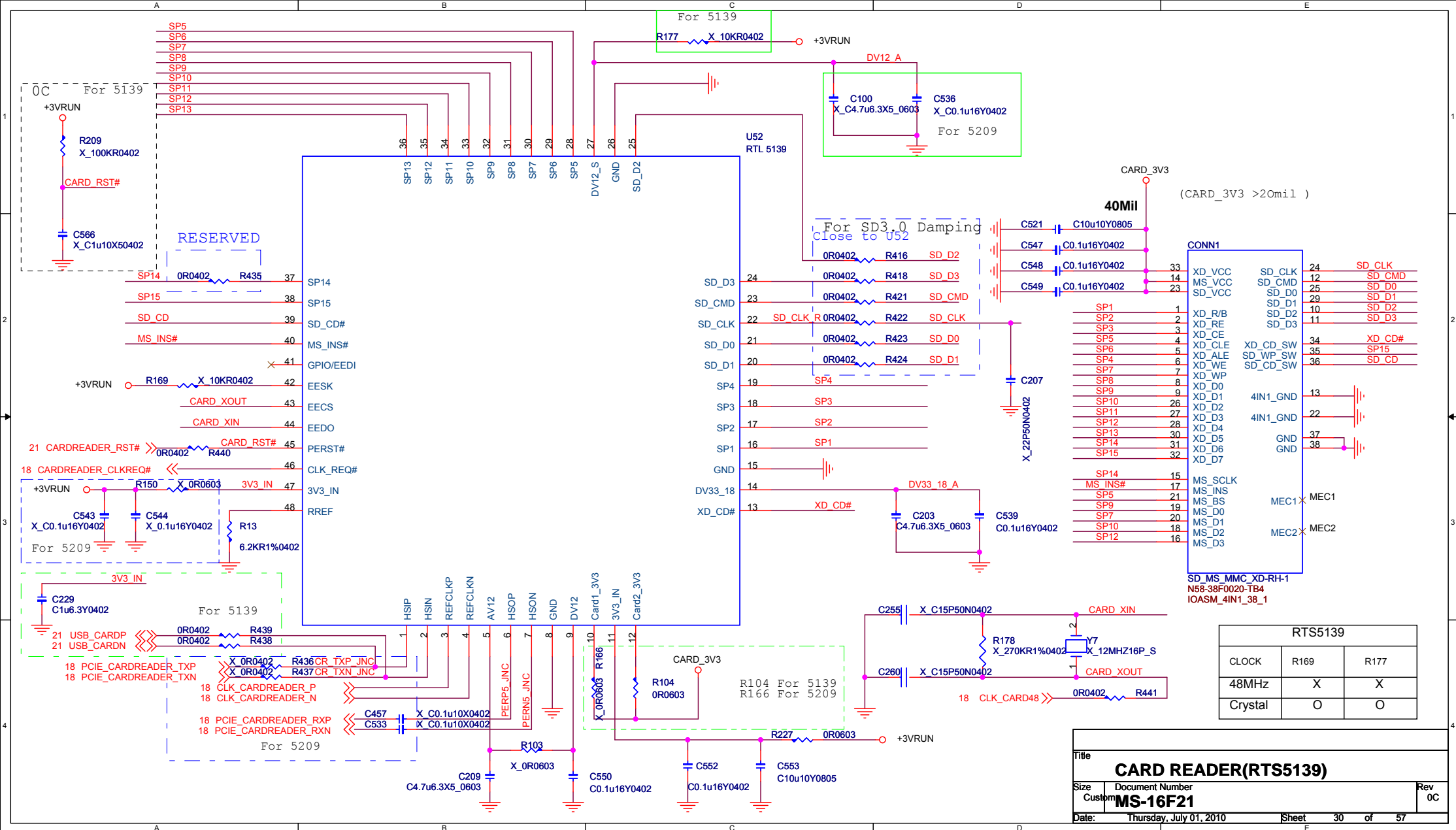


**MSI** MICRO-STAR INT'L CO.,LTD.

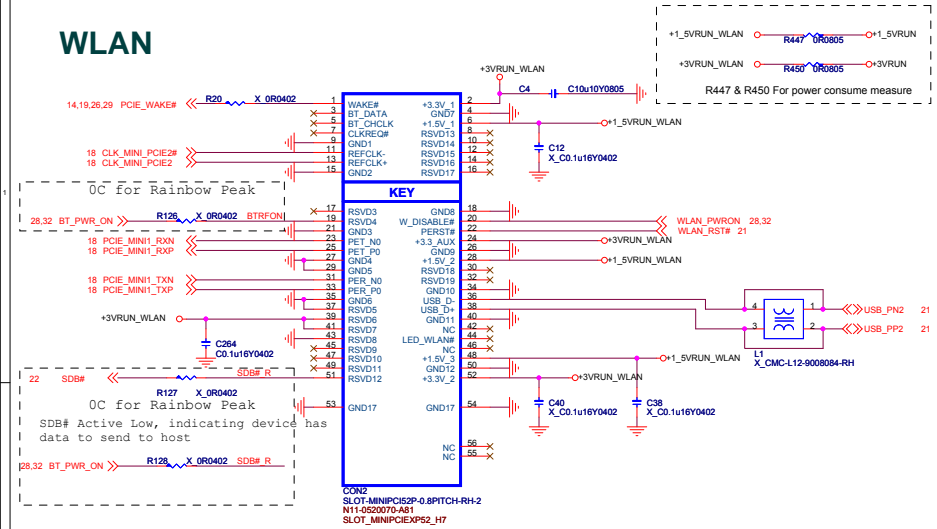
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Size: Custom Document Number: **MS-16F21**

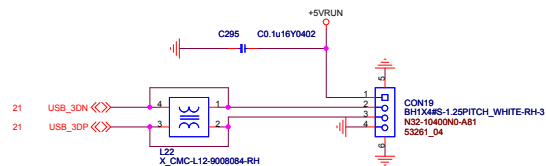
Date: \_\_\_\_\_ Sheet: 29 of 57



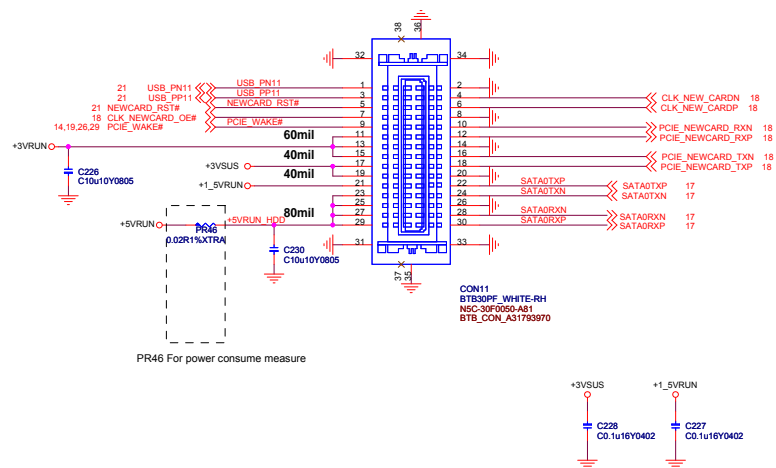
## WLAN



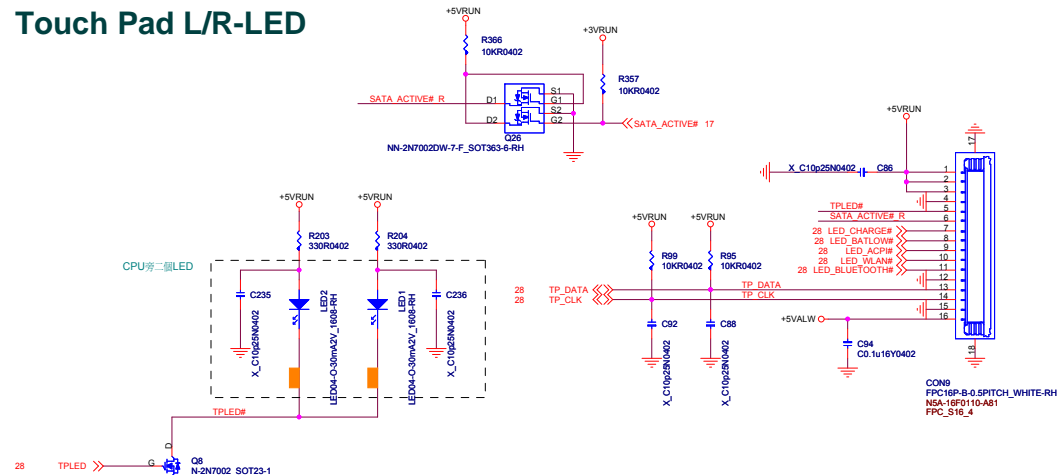
## 3D glass



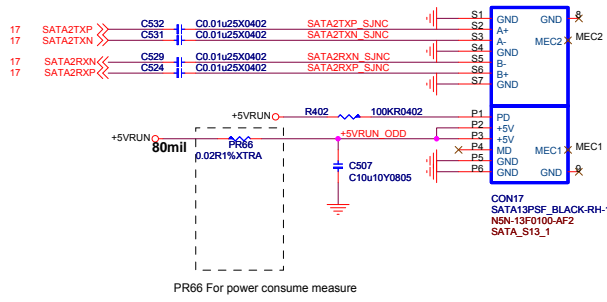
## BTB Conn



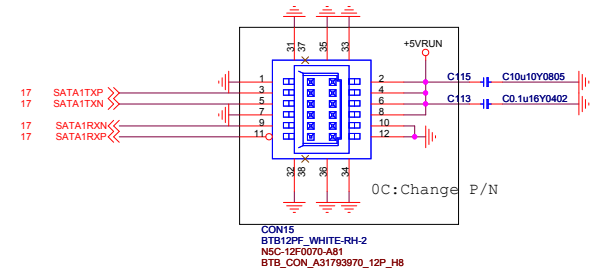
## Touch Pad L/R-LED



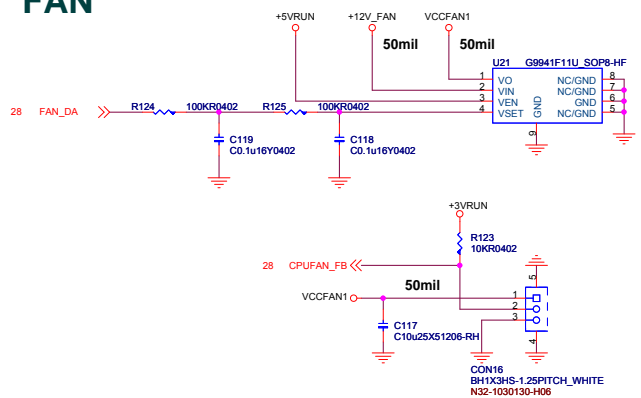
ODD



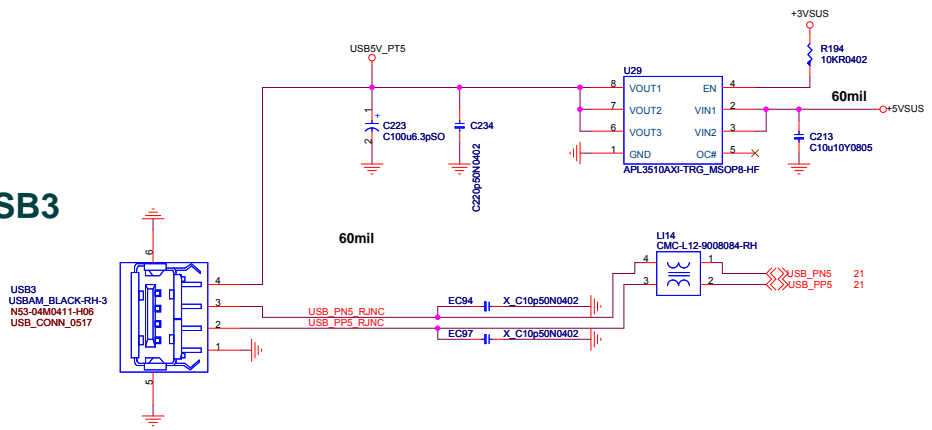
SATA HDD2



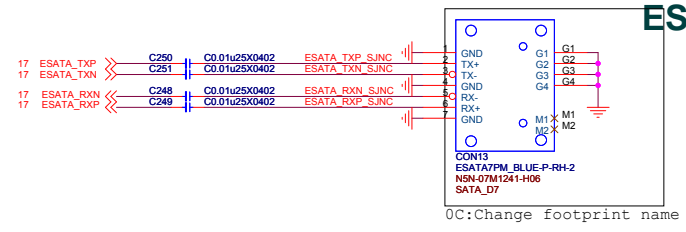
FAN



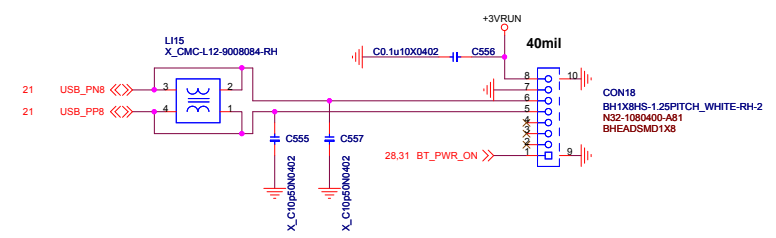
USB3



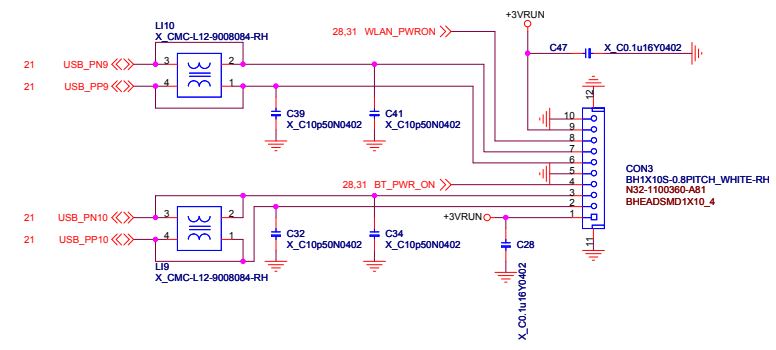
ESATA



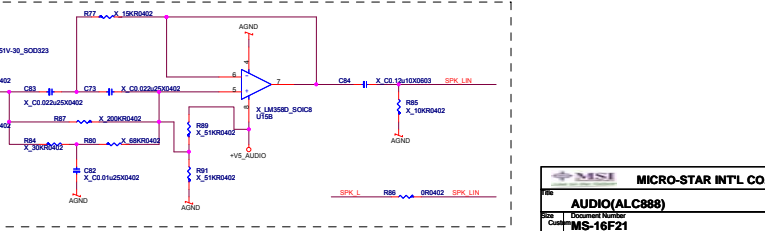
BT (3801)

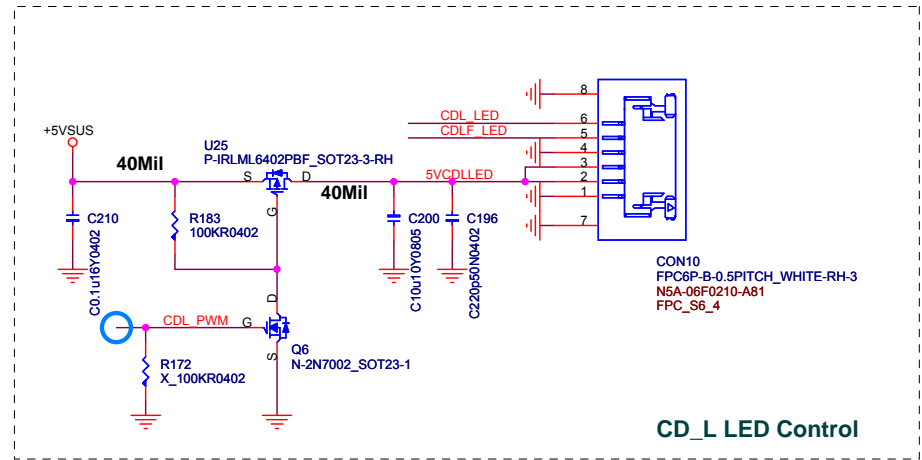
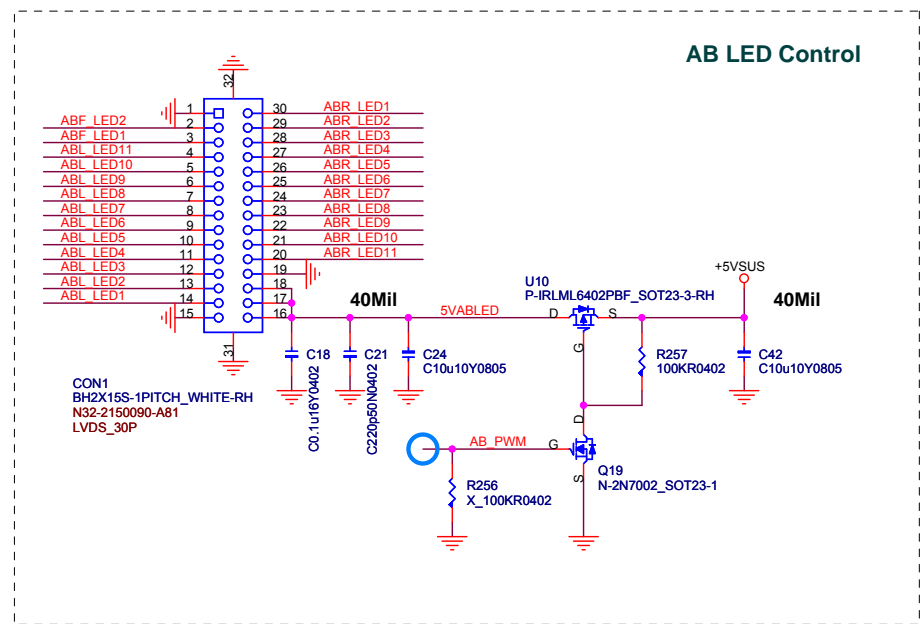
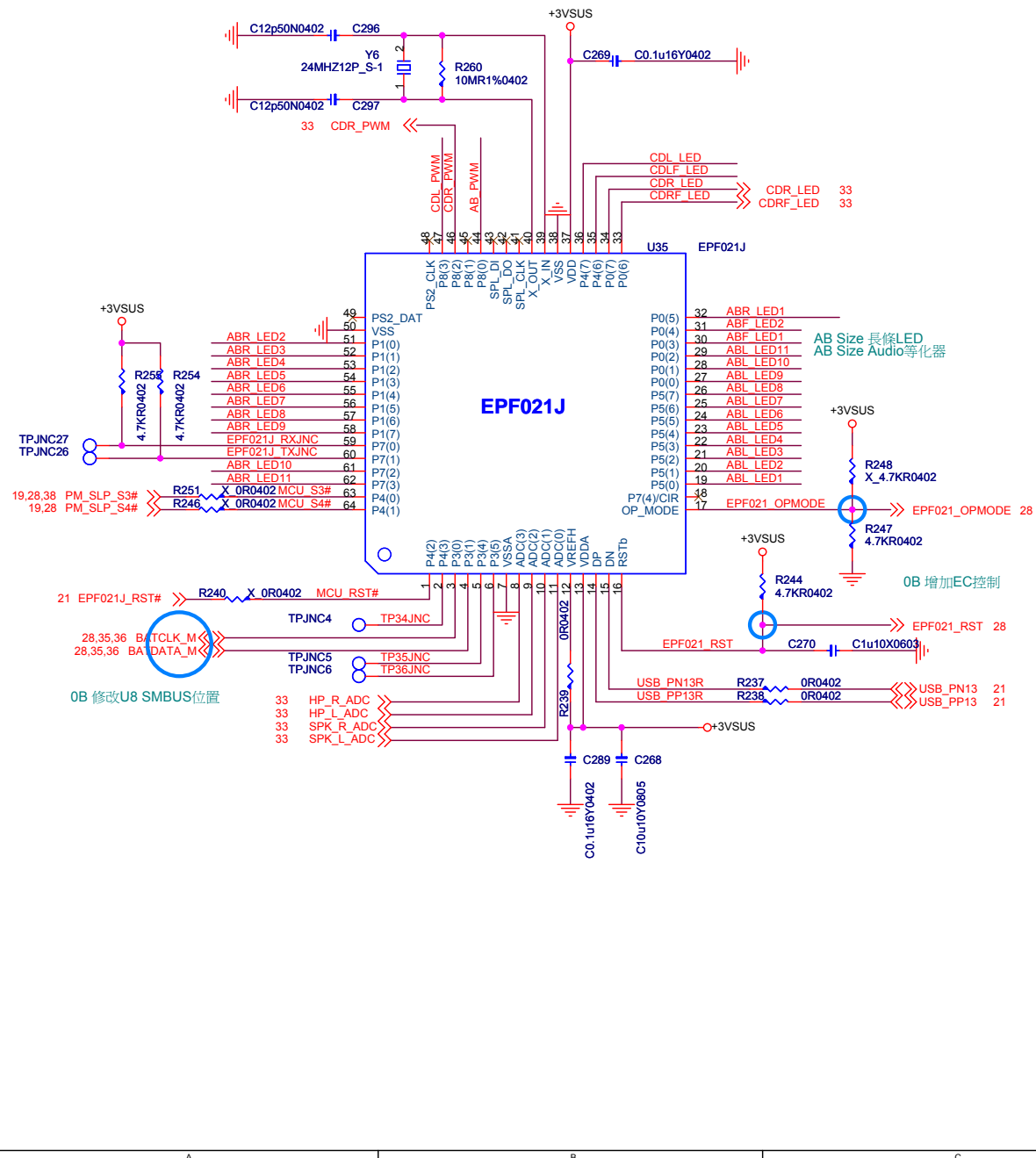


WLAN/BT (3870)

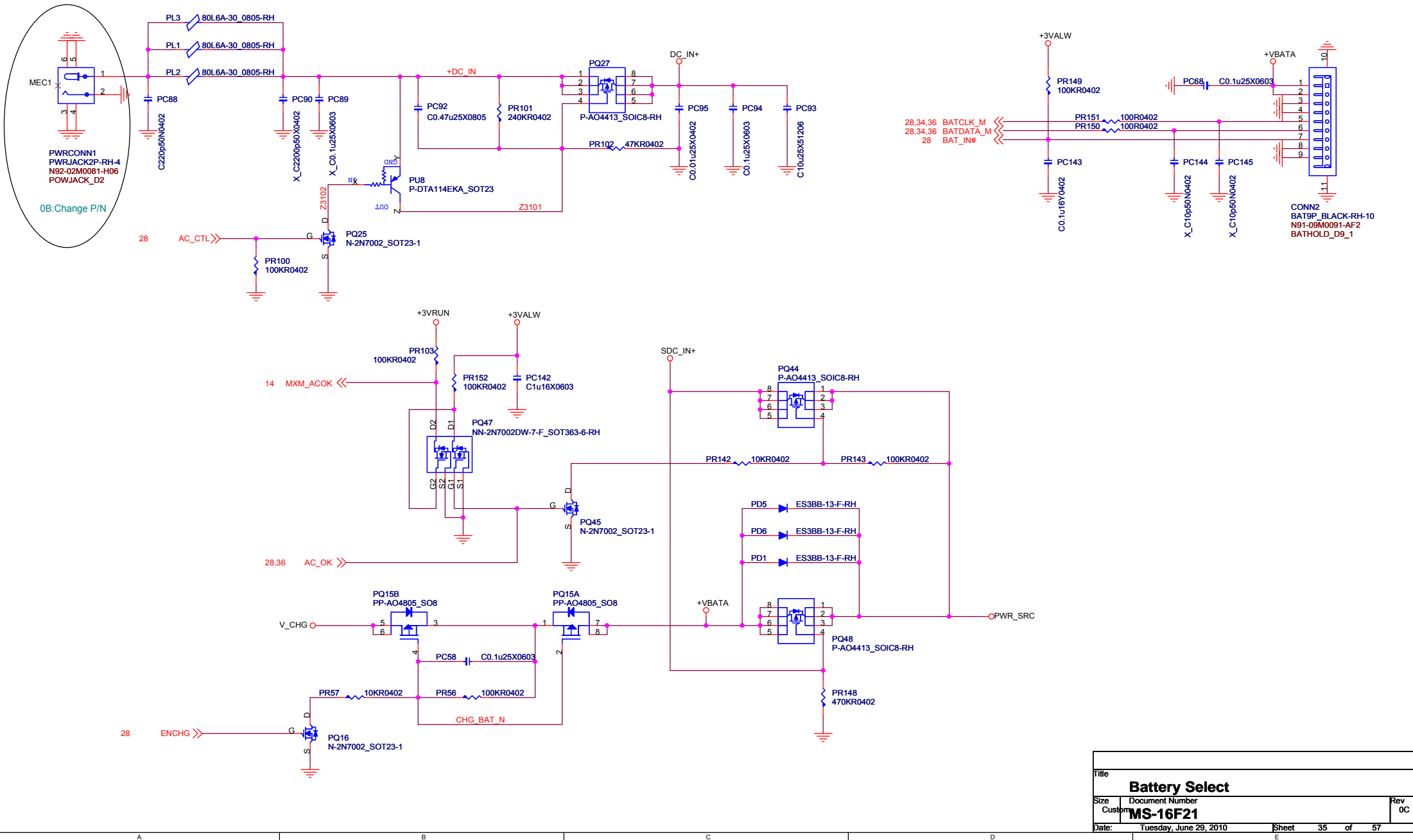




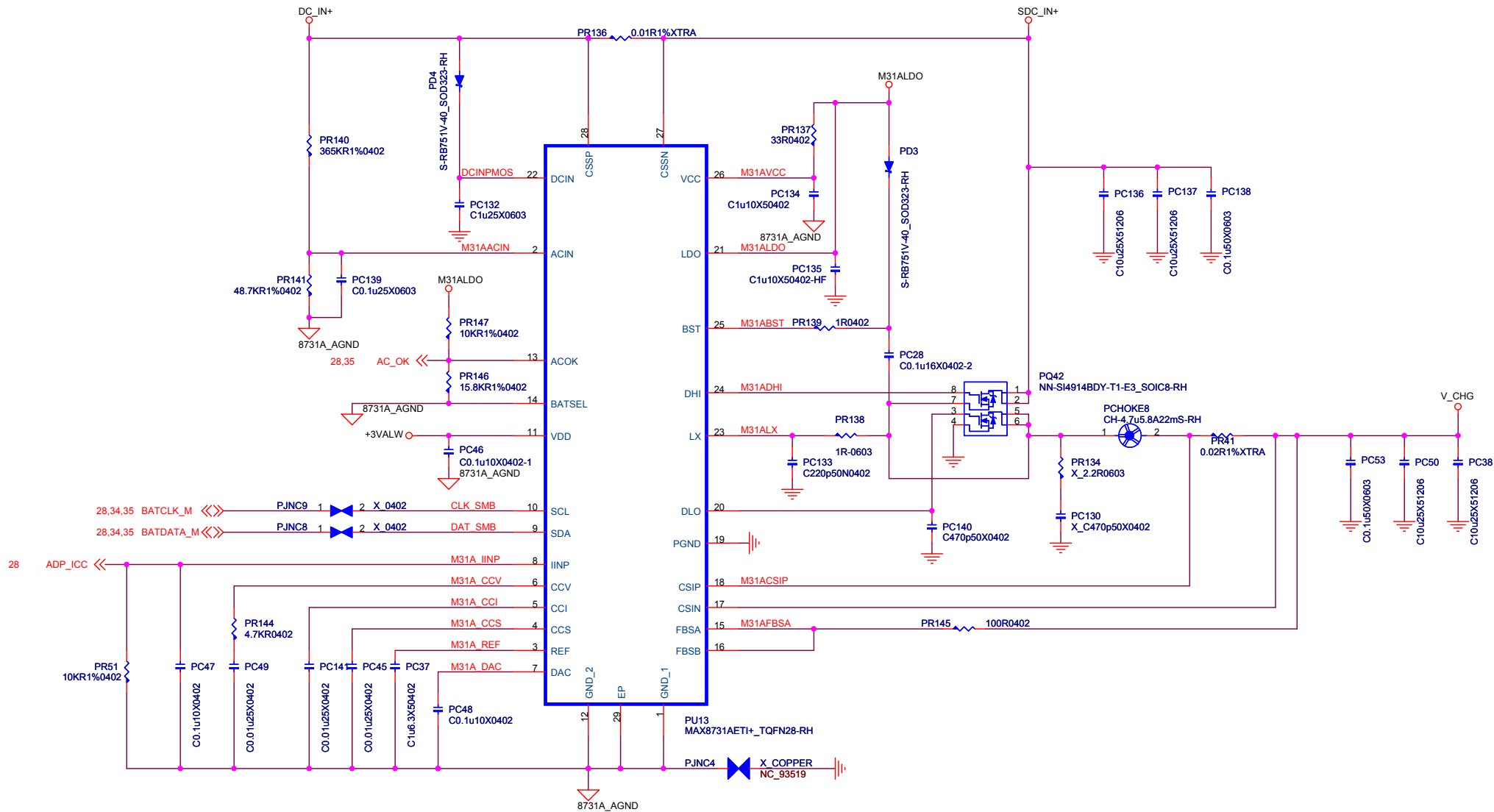




Title		
EPF021J		
Size	Document Number	Rev
B	MS-16F21	0C
Date:	Tuesday, June 29, 2010	Sheet 34 of 57



Title			
Battery Select			
Size	Document Number		Rev
Custom	MS-16F21		0C
Date:	Tuesday, June 29, 2010	Sheet	35 of 57



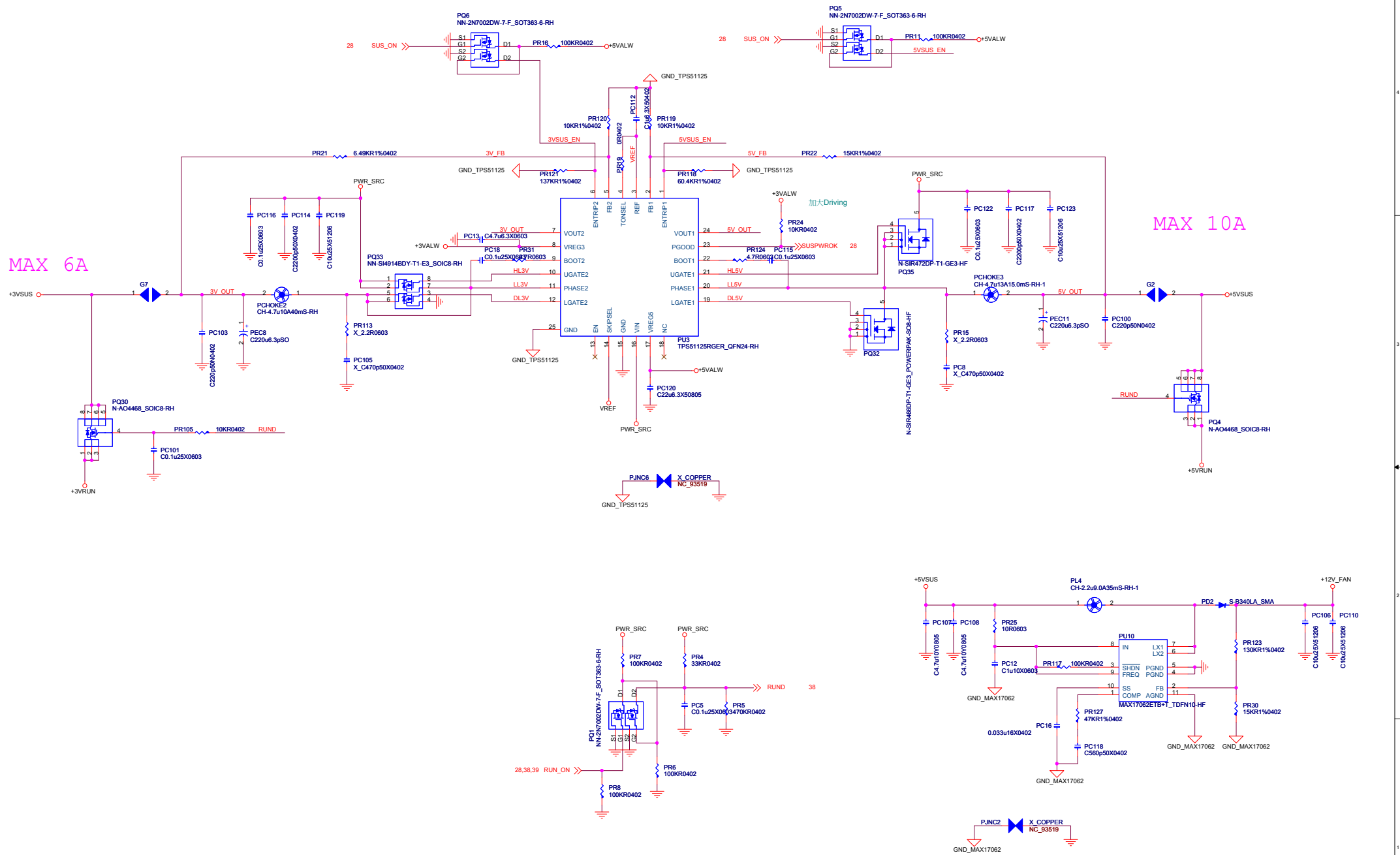
IINP :

1. The transconductance from (CSSP - CSSN) to IINP is 3mA/V.
2.  $V\_IINP = IINPUT \times RS1 \times 3mA/V \times PR168$

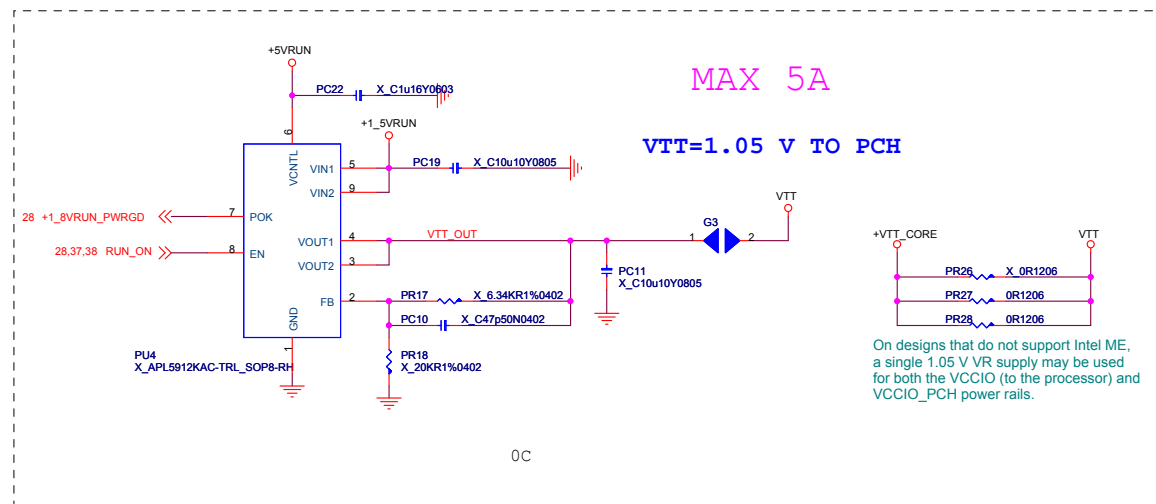
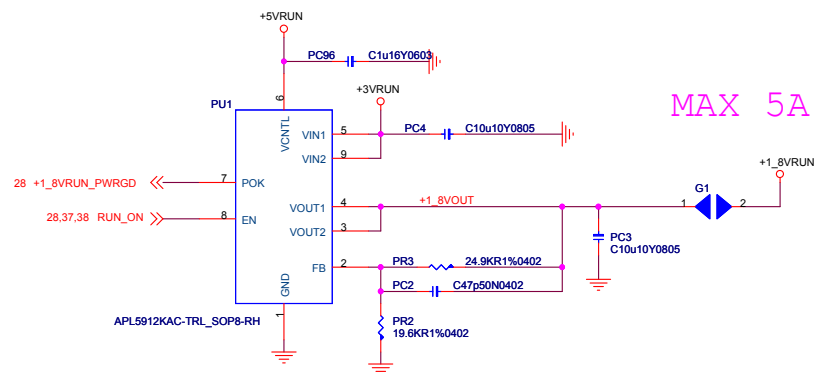
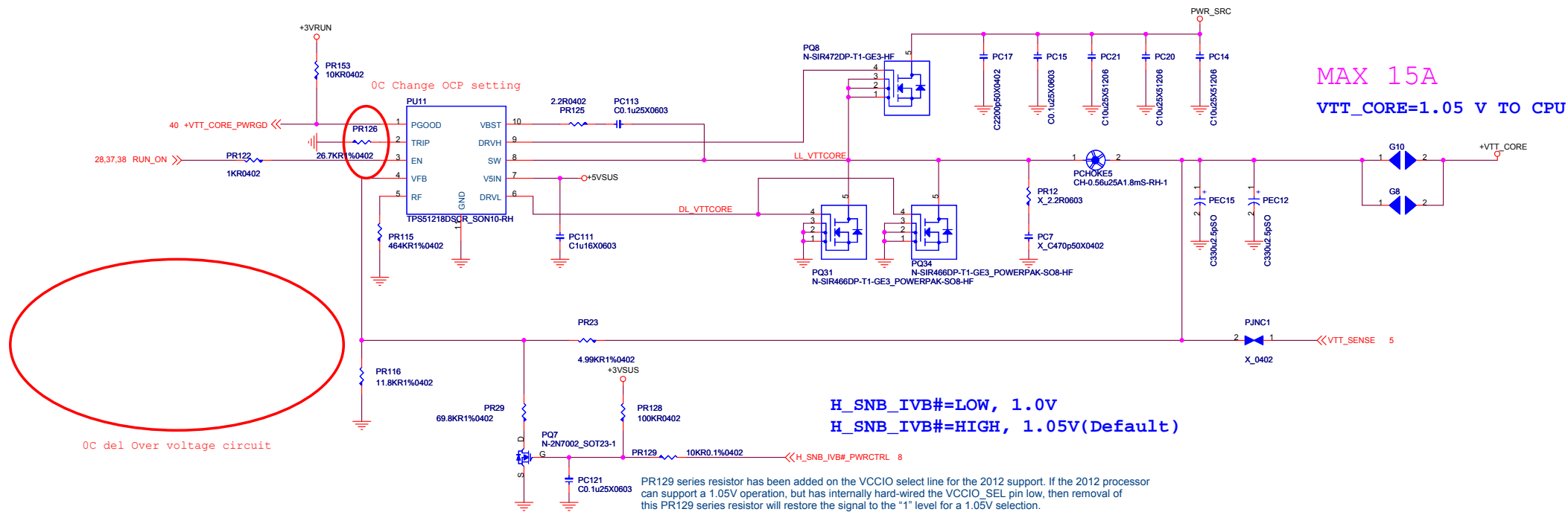
Title		
Battery Charger		
Size	Document Number	Rev
B	MS-16F21	0C
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MAX 6A

MAX 10A





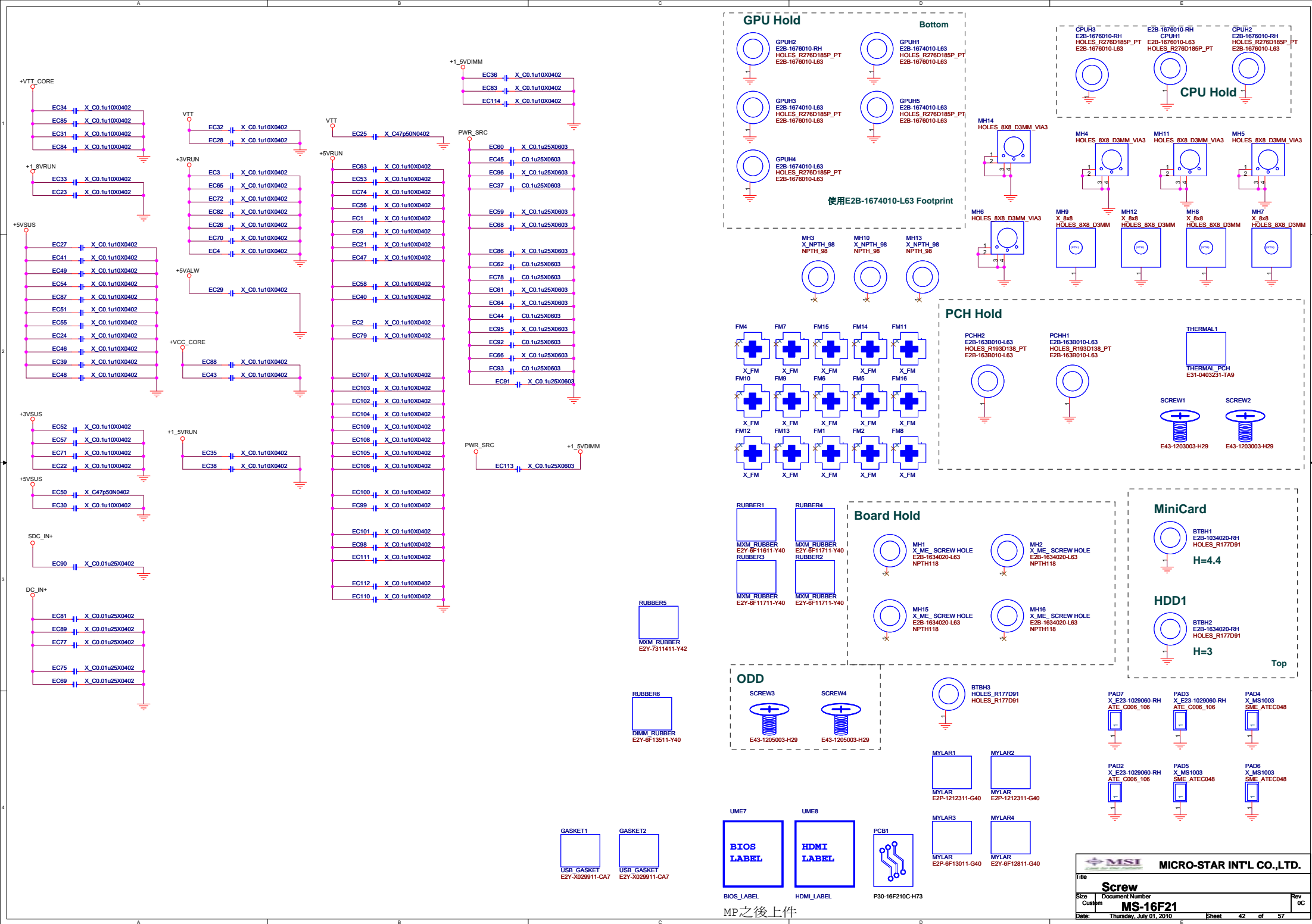


Title			VTT_1.8VRUN	
Size	Custom	Document Number	MS-16F21	
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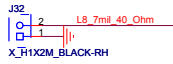
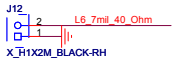
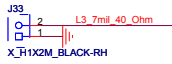
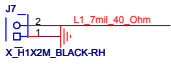




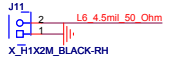
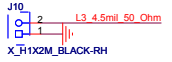




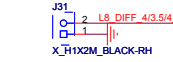
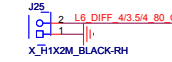
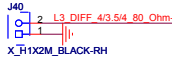
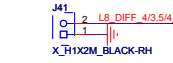
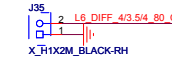
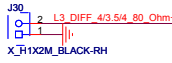
40 OHM



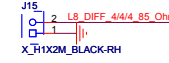
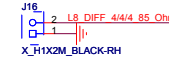
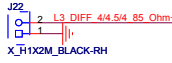
50 OHM



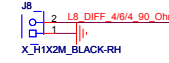
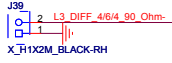
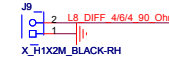
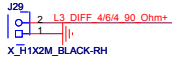
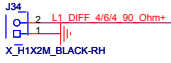
80 OHM



85 OHM



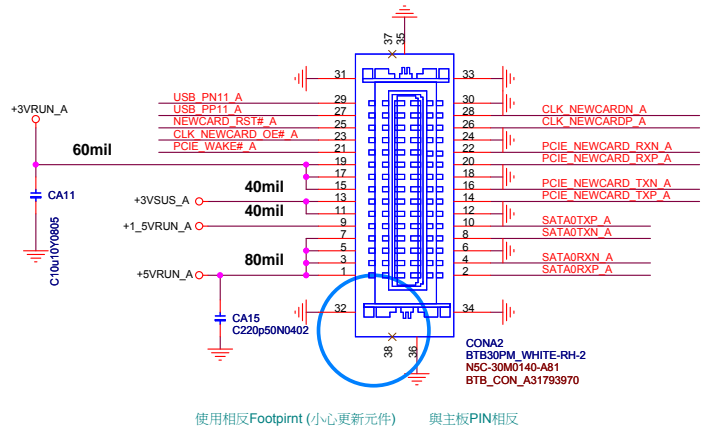
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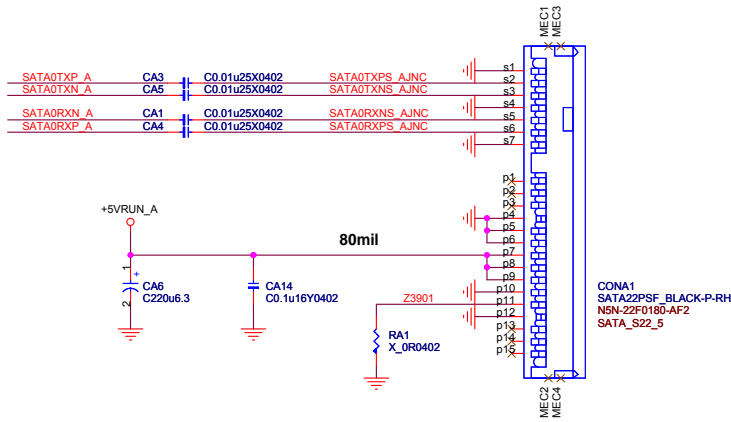
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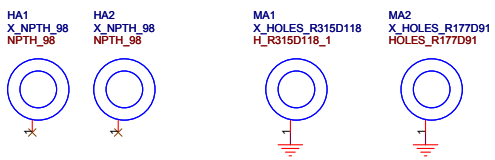
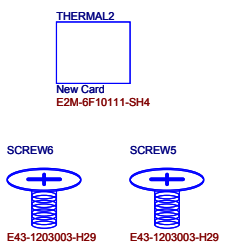
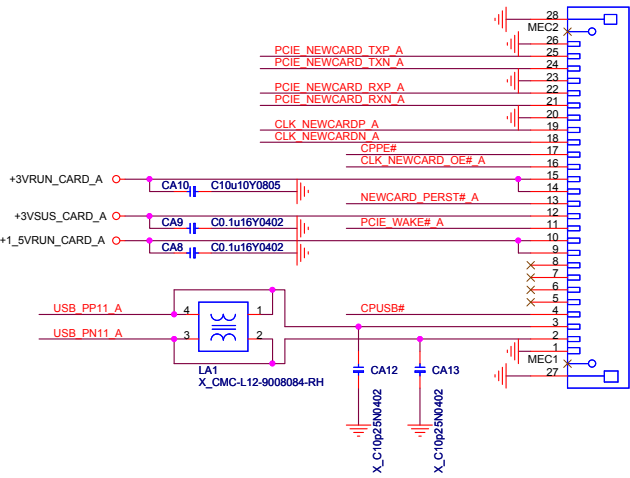
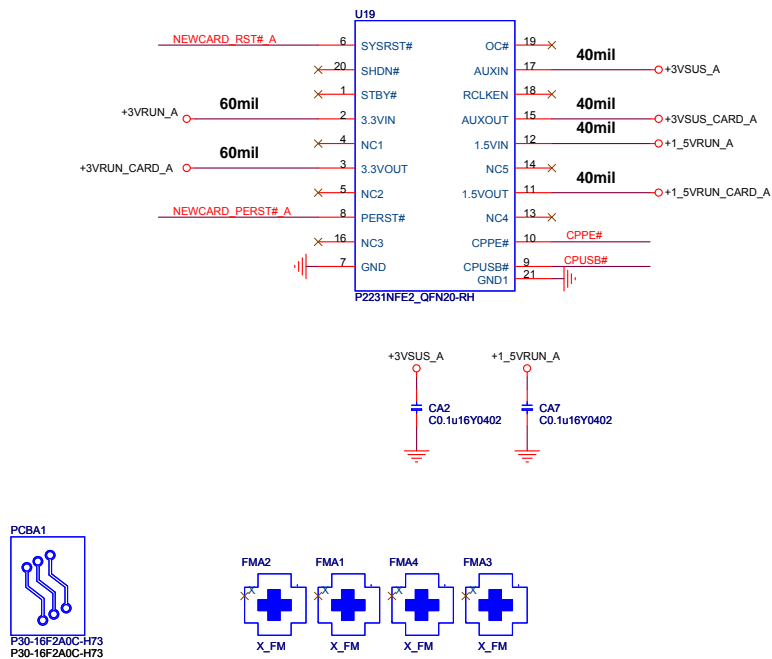
BTB Conn



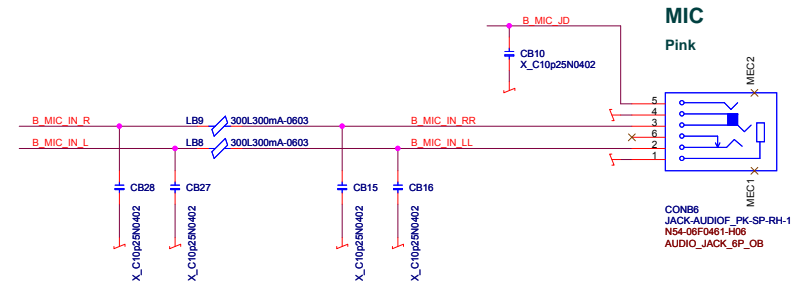
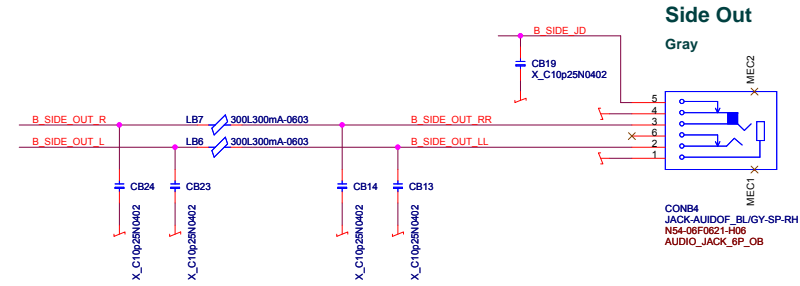
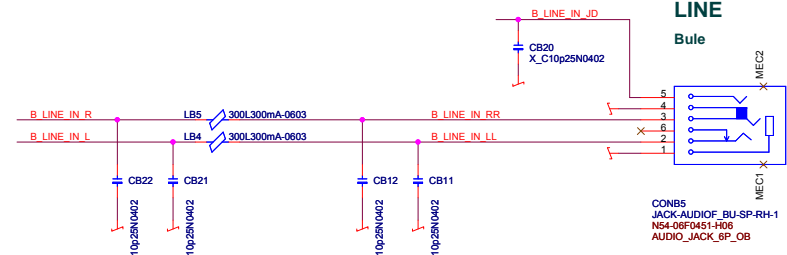
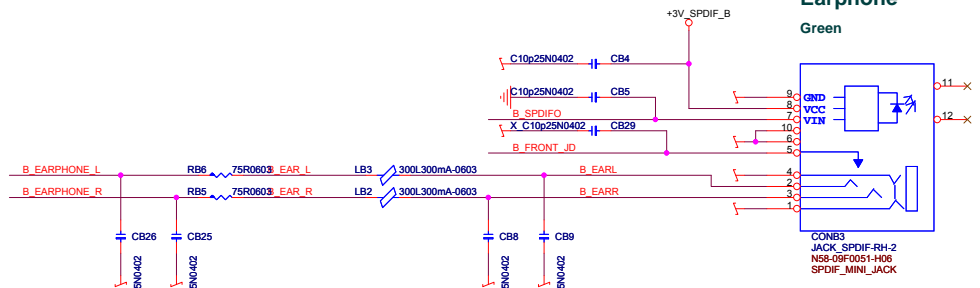
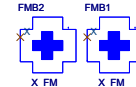
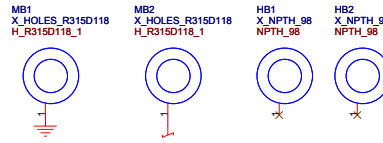
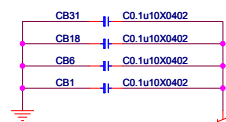
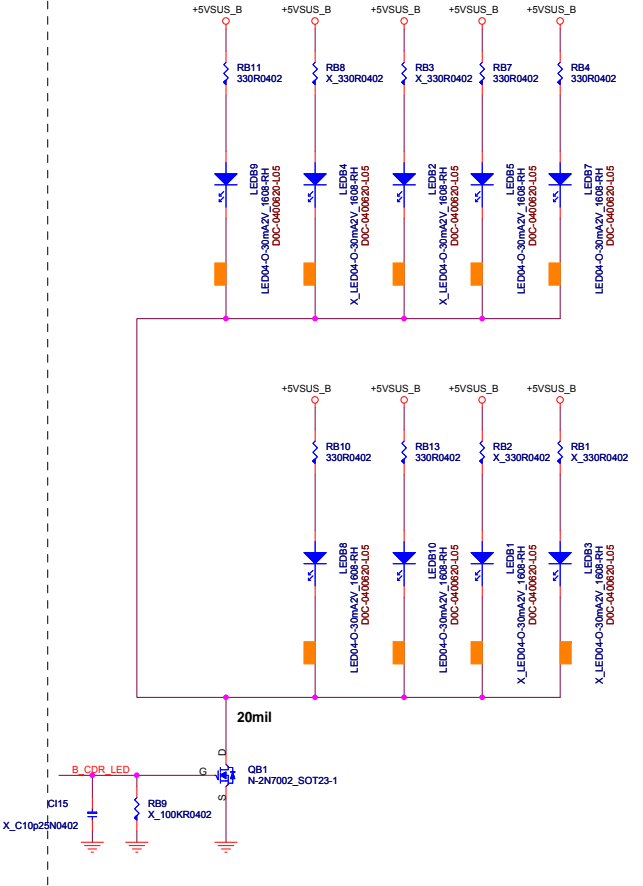
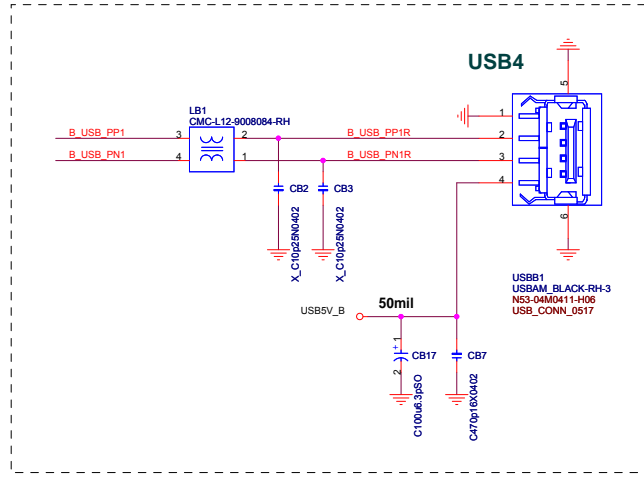
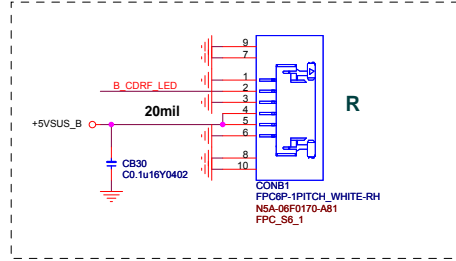
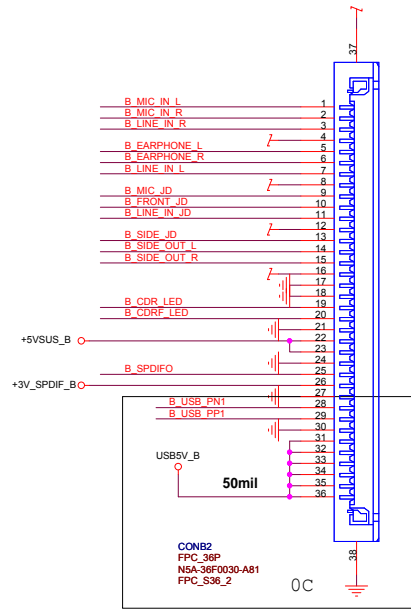
SATA HDD1

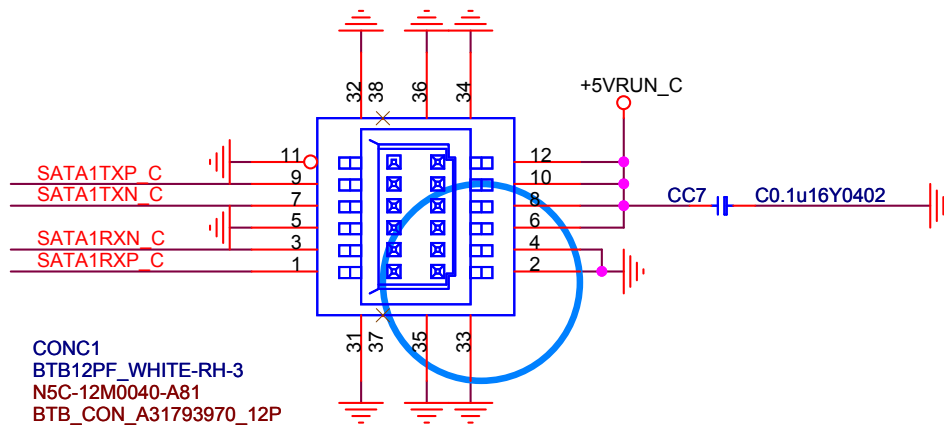


NewCard



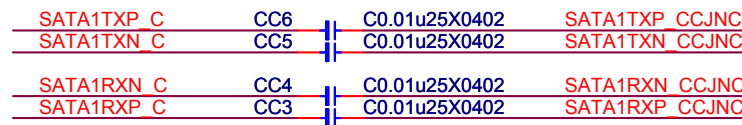
MSI Micro-Star International Co., Ltd.			
Title NewCard/HDD			
Size	Document Number	Rev	
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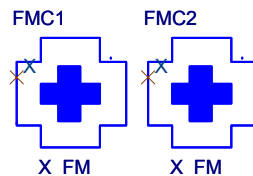
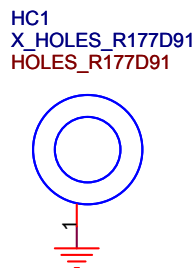
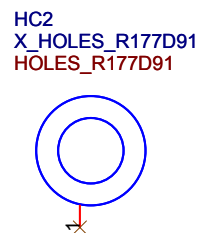
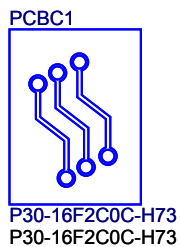
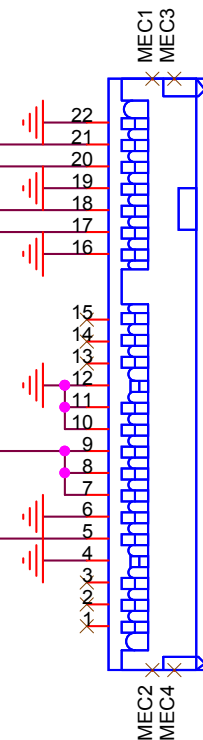
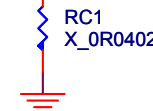
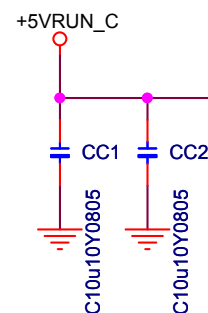


使用相反Footprint (小心更新元件)

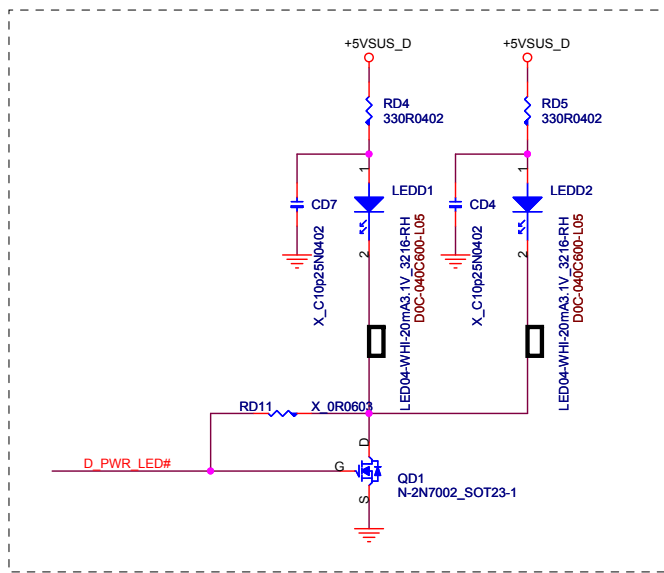
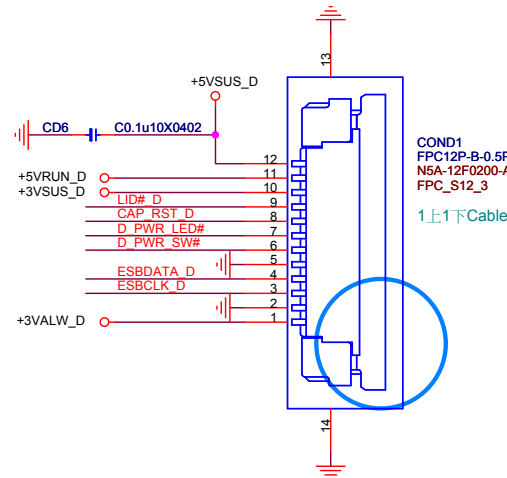
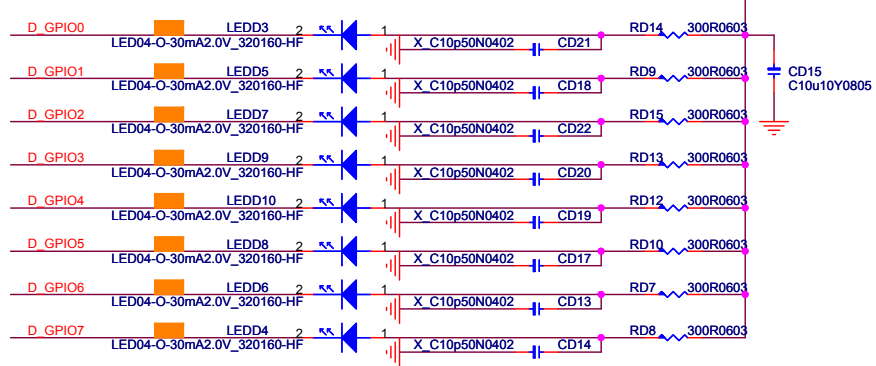
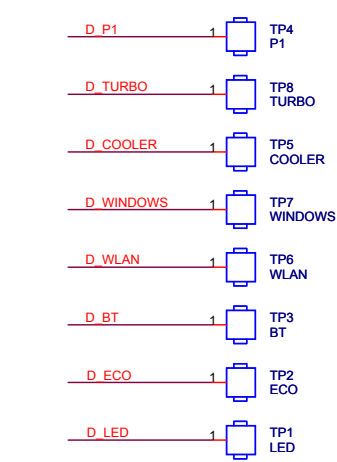
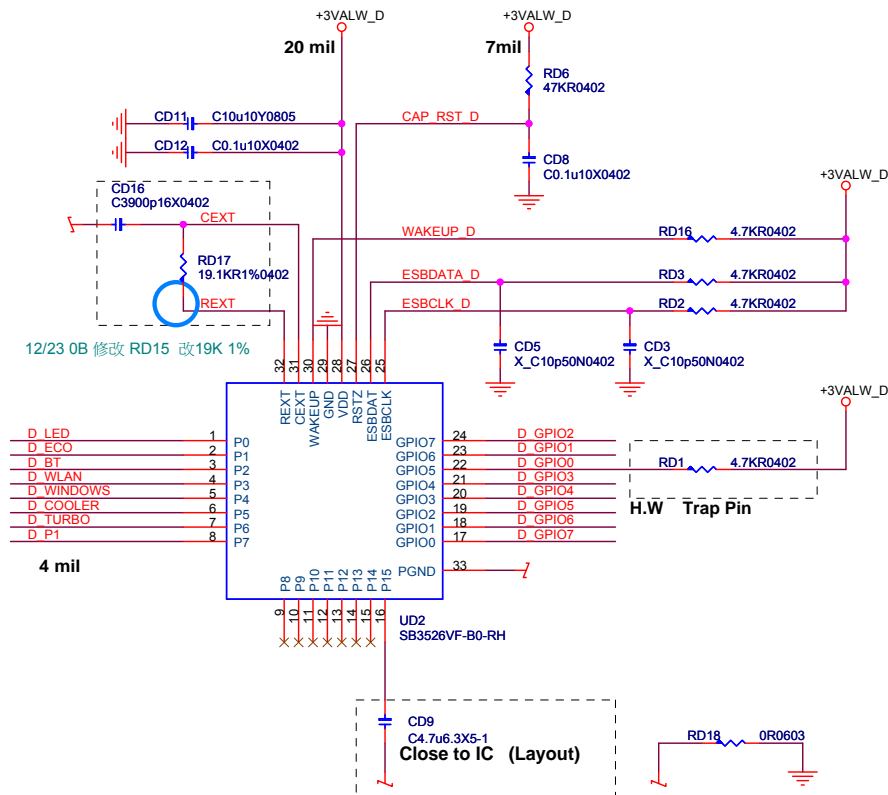
與主板相反



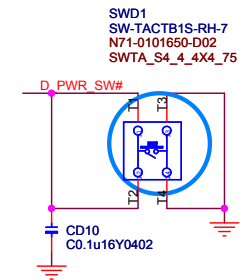
CONC2  
SATA2PSF\_BLACK-P-RH-3  
N5N-22F0210-A81  
SATA\_S22\_8



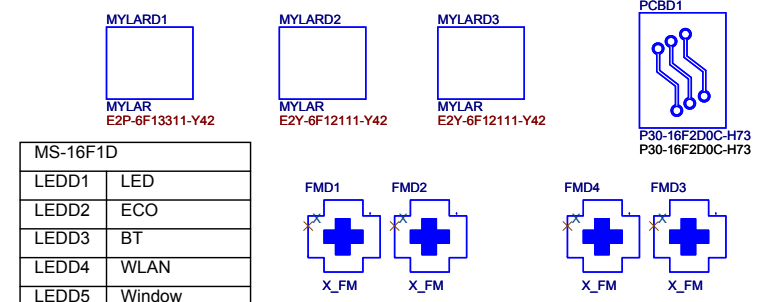
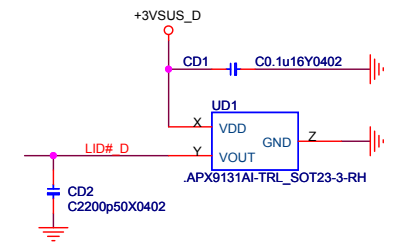
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Title <b>HDD2</b>		
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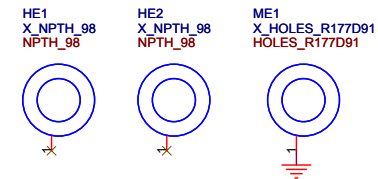
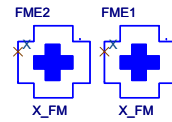
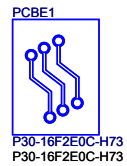
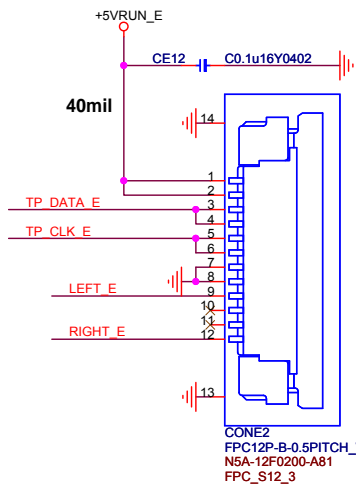
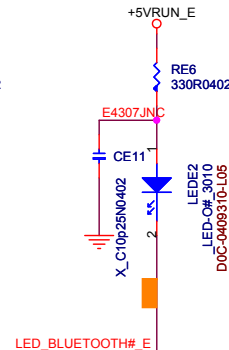
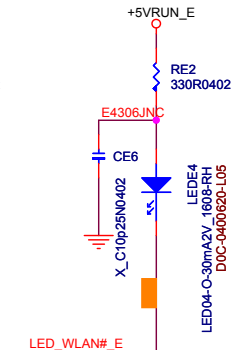
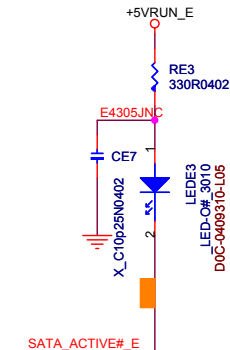
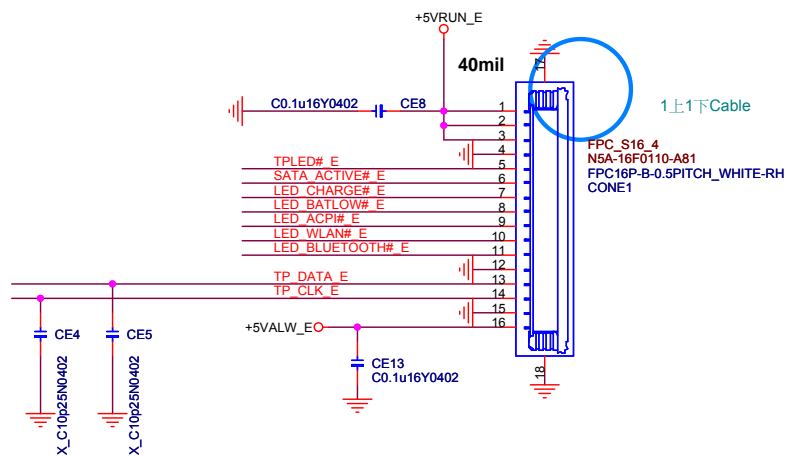
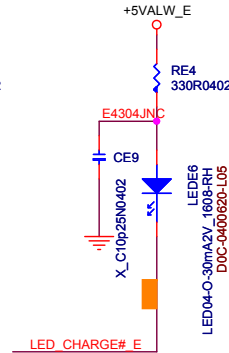
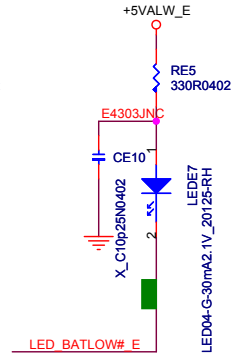
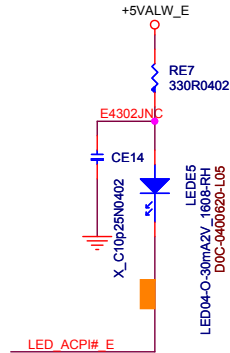
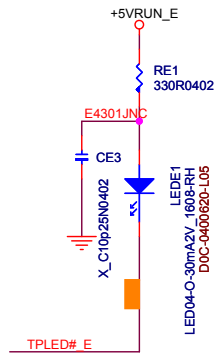
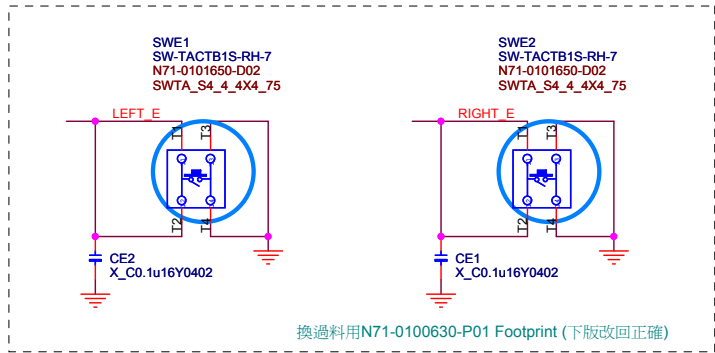
## Power Switch



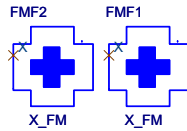
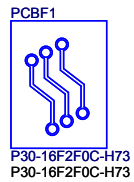
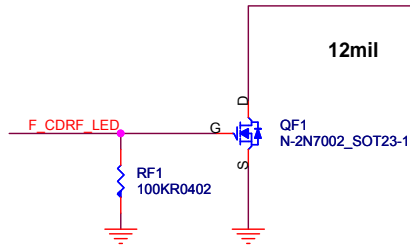
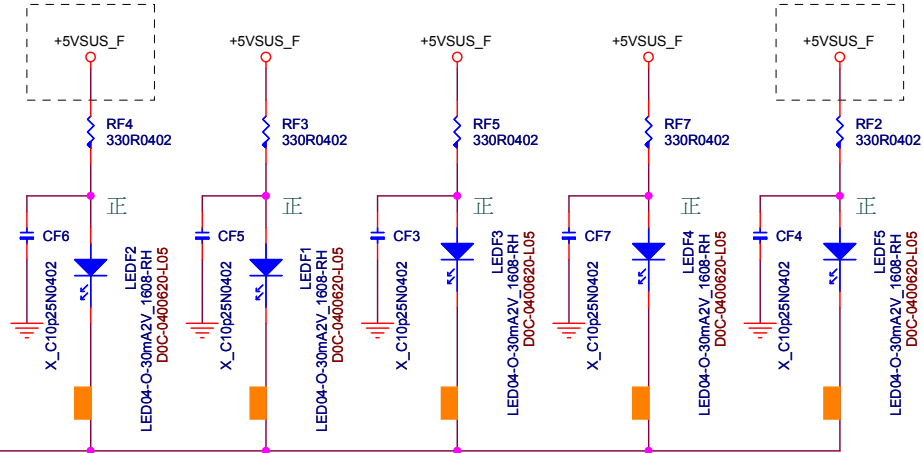
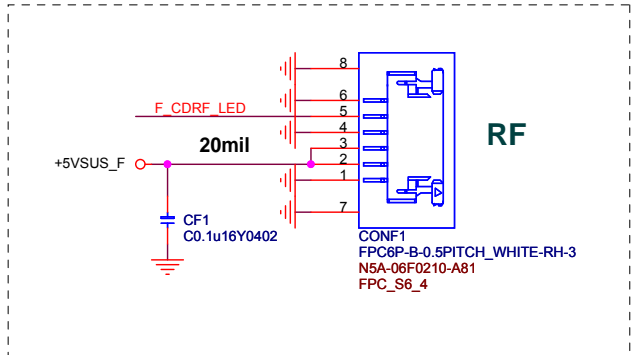
## Hall Sensor




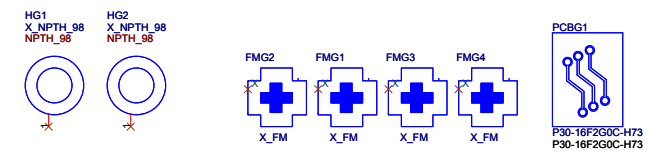
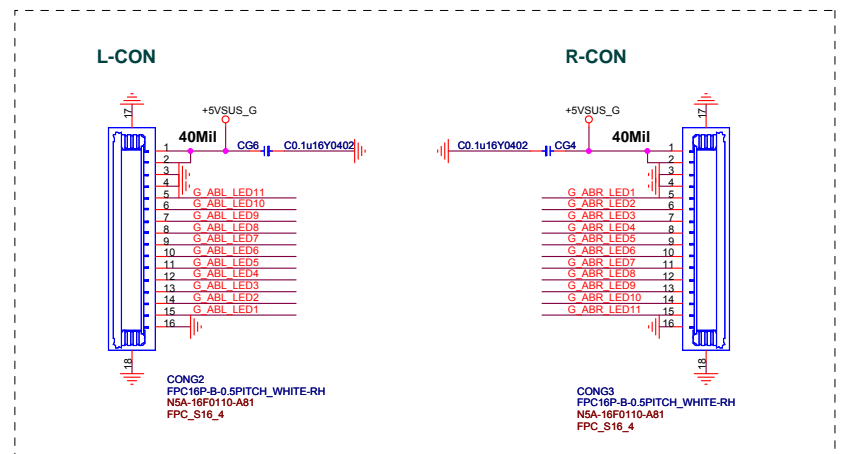
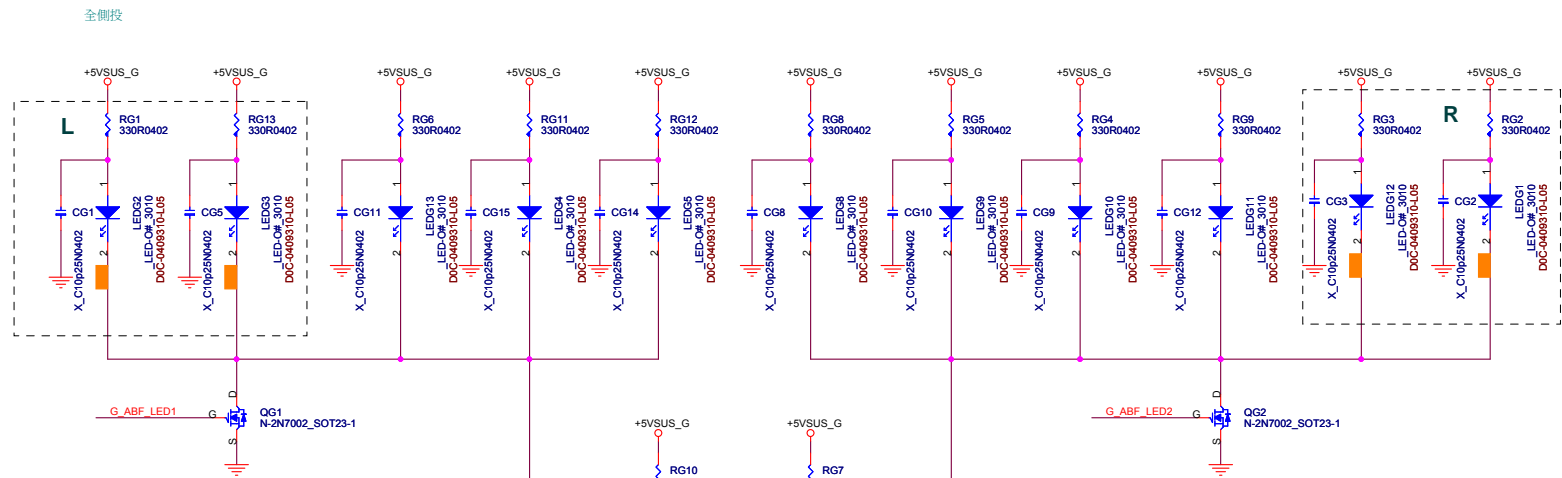
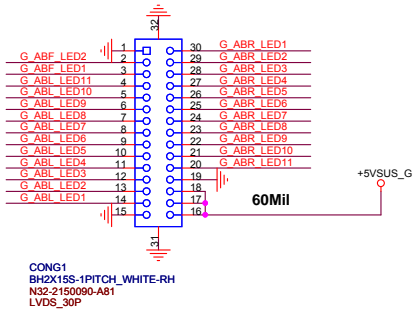
MS-16F1D	
LEDD1	LED
LEDD2	ECO
LEDD3	BT
LEDD4	WLAN
LEDD5	Window
LEDD6	COOLER
LEDD7	TURBO
LEDD8	P1



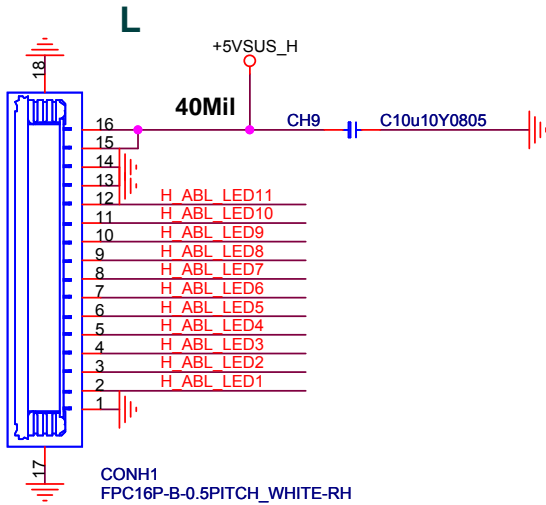




 <b>MICRO-STAR INT'L CO.,LTD.</b>		
Title <b>CDLED_RF</b>		
Size Custom	Document Number <b>MS-16F2F</b>	Rev 0C
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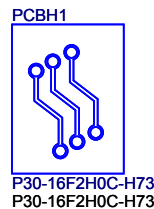
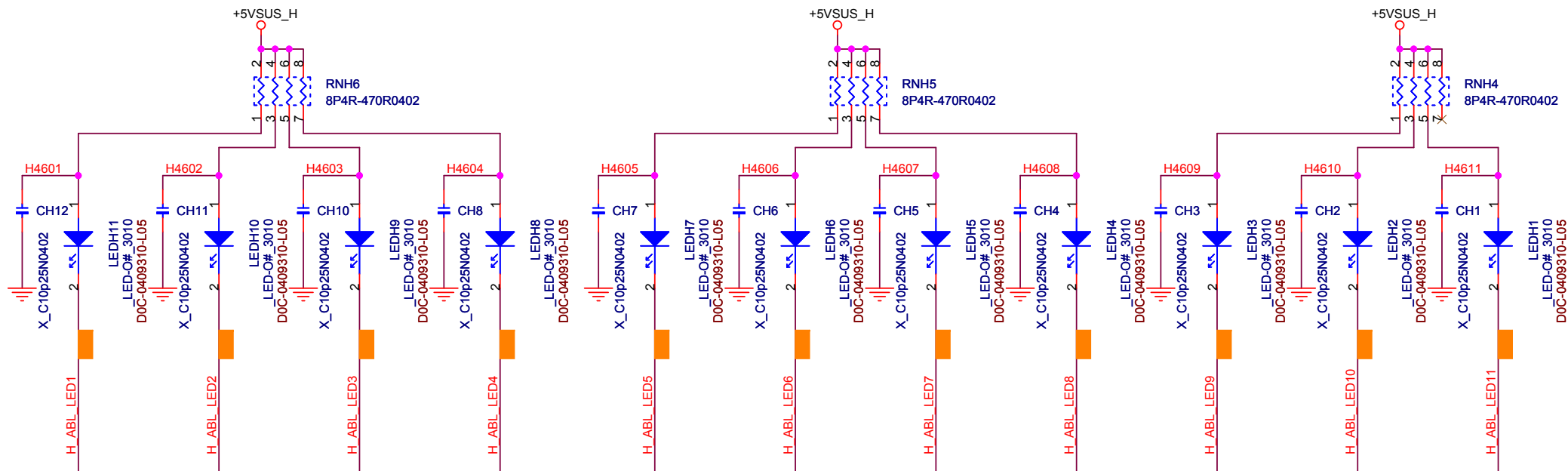


Title			
AB Size LED_F			
Size	Document Number		Rev
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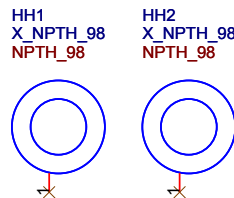


CONH1  
FPC16P-B-0.5PITCH\_WHITE-RH  
N5A-16F0110-A81  
FPC\_S16\_4

全側投



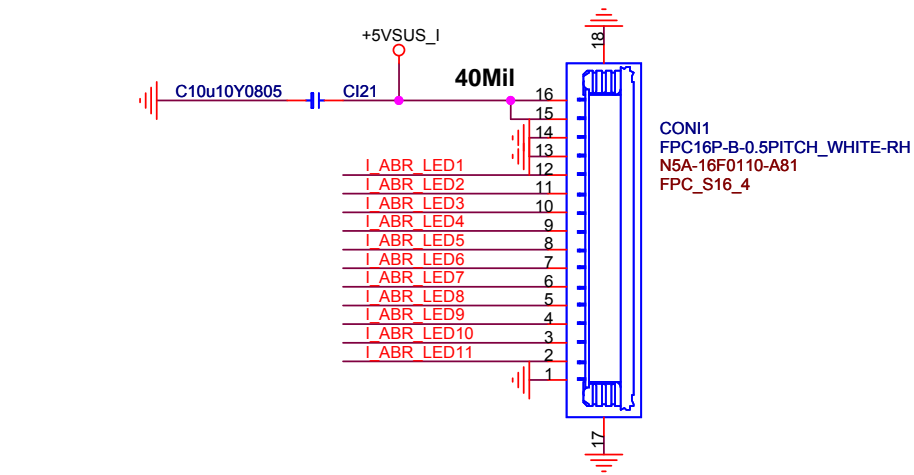
P30-16F2H0C-H73  
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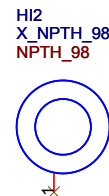
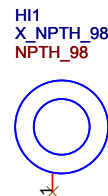
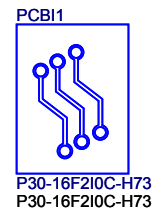
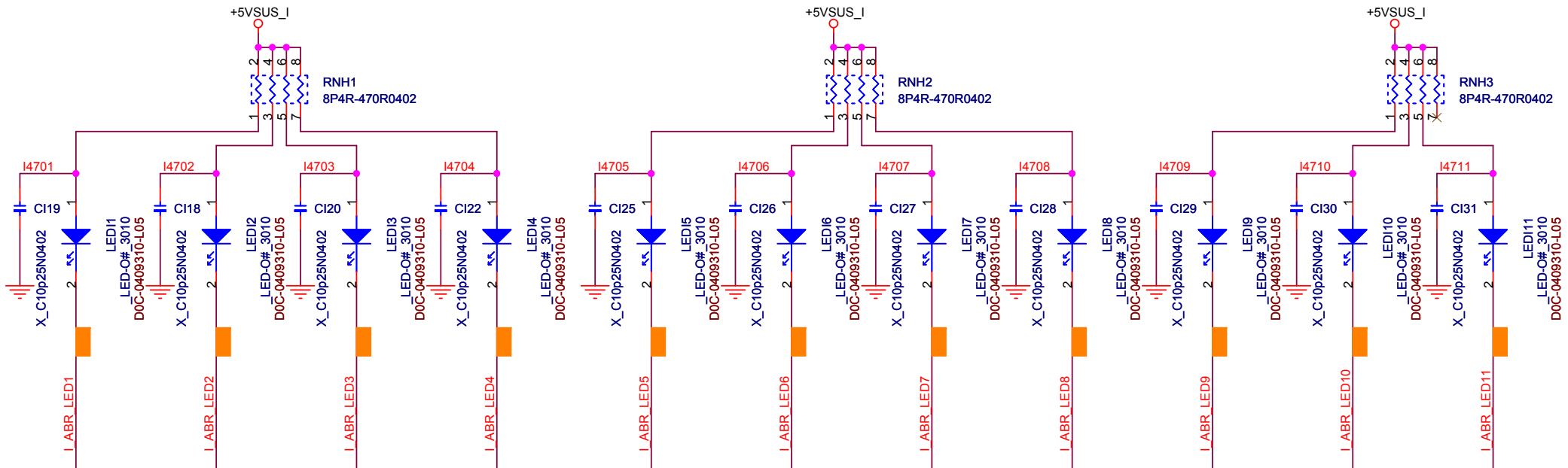
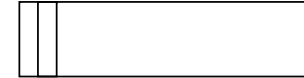
HH1  
X\_NPTH\_98  
NPTH\_98

HH2  
X\_NPTH\_98  
NPTH\_98

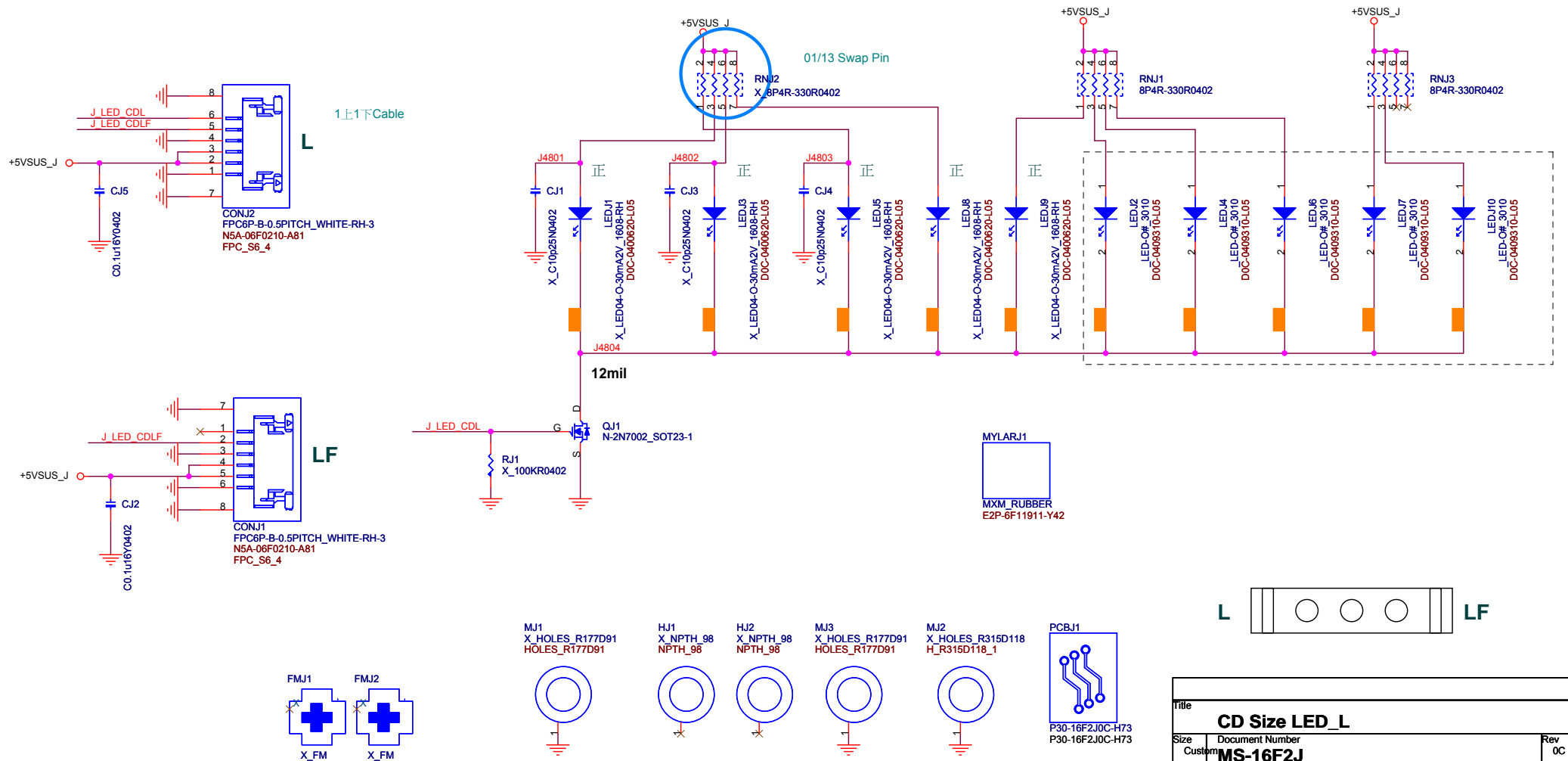
Title		
AB Size LED_L		
Size	Document Number	Rev
Custom	MS-16F2H	0C
Date:	Thursday, July 01, 2010	Sheet 51 of 57



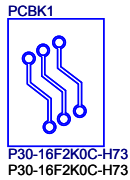
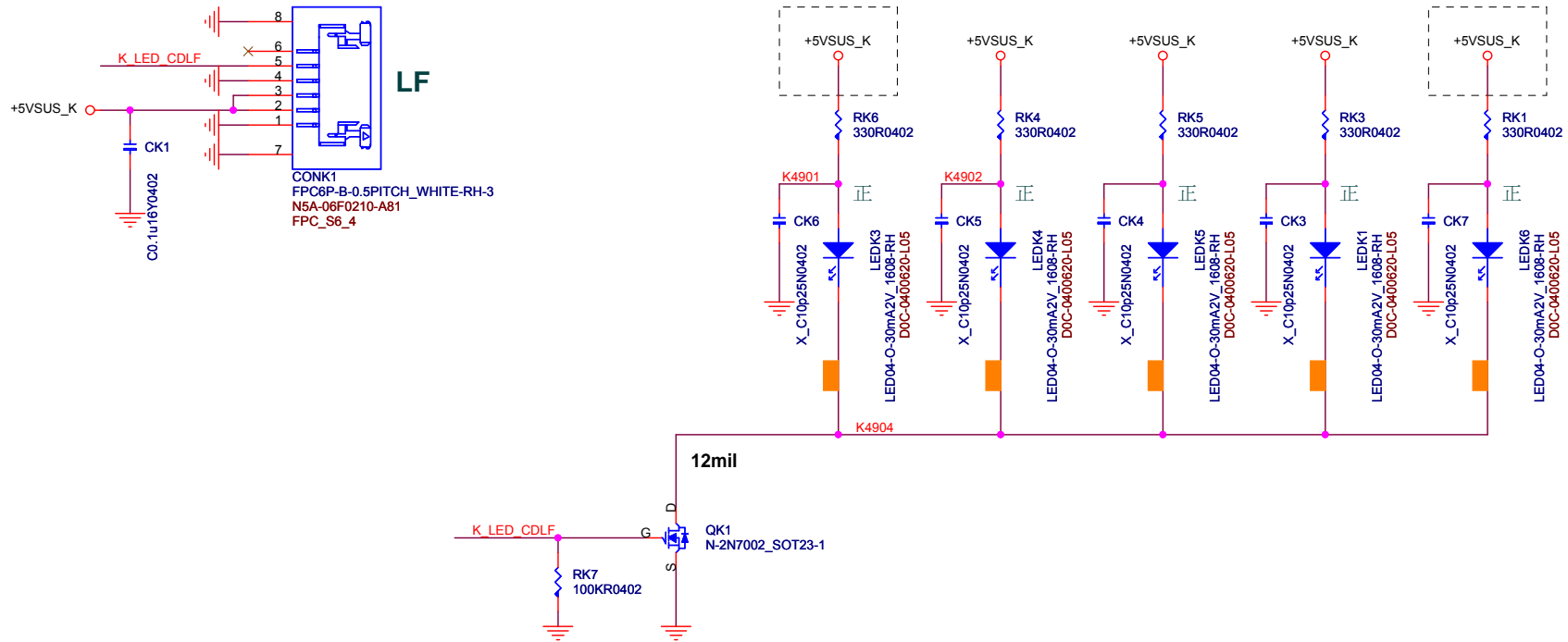
R



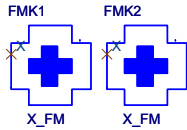
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AB Size LED_R		
Size	Document Number	Rev
Custom	MS-16F21	0C
Date:	Thursday, July 01, 2010	Sheet 52 of 57



Title				
<b>CD Size LED_L</b>				
Size	Document Number			Rev
Custom	<b>MS-16F2J</b>			OC
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P30-16F2K0C-H73  
P30-16F2K0C-H73



FMK1  
X\_FM

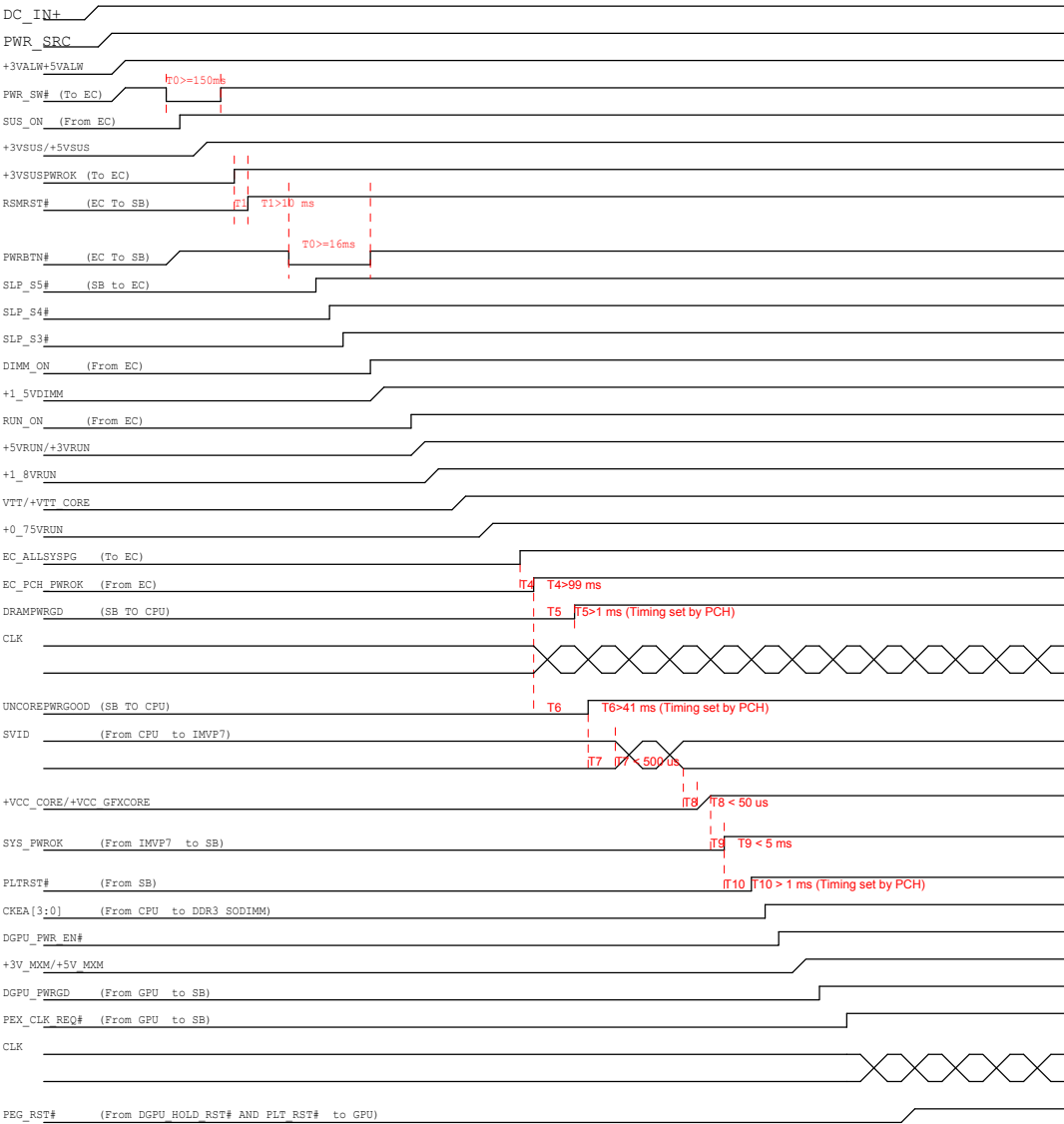
FMK2  
X\_FM

LF



Title		
CD Size LED_LF		
Size	Document Number	Rev
Custom	MS-16F2K	0C
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S5-S0  
EC programming timing  
Intel Huron River timing SPEC



Power down Sequence DC mode S0 to G3

S0-S5  
EC programming timing  
Intel Huron River timing SPEC

